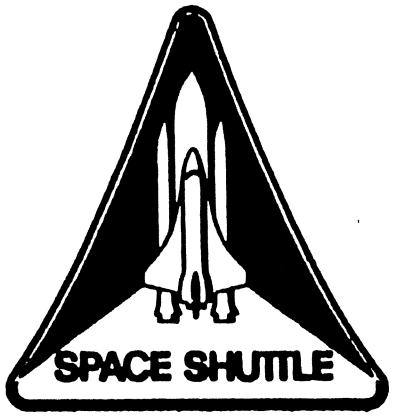


SSME
BLOCK II CONTROLLER

Rockwell
International
Rocketdyne Division

Creation of the Block II Controller

The Block II Controller was created primarily due to parts obsolescence in the existing Block I SSME Controller. In 1980, Signetics discontinued production of the 8000 series logic microchips. The series 8000 is the main logic family in use on the Block I. By 1982, 37 of the 266 electrical part types had become commercially unavailable. This trend continued so that by 1985 over 30% (80 parts) were unavailable.

In September 1982, Honeywell proposed the inception of the Block II Controller in order to address this issue of parts obsolescence.

Block II Program Milestones

September 17, 1982
Honeywell submitted a formal change proposal for the Block II Controller

September 29, 1983
Rocketdyne approved Honeywell's change proposal and issued a purchase order

January 23, 1984
Block II Controller ECP 704 Basic approved by MSFC

September 5, 1984
Preliminary Design Review (PDR) held at Honeywell with 47 Review Item Discrepancies (RID's) generated - all have been closed

September 10, 1985
Critical Design Review (CDR) held at Honeywell with 24 RID's generated - all have been closed

January 24, 1986
Block II Controller Brassboard unit #1 shipped in place to Honeywell

February 27, 1986
Block II Controller Brassboard unit #2 shipped to Rocketdyne Canoga Software Lab (CSL) for software development

December 5, 1986
Block II Controller Brassboard unit #3 shipped to Huntsville Simulation Lab (HSL) for software testing

May 1, 1989
Block II Controller completed Qualification Testing

June 30, 1989
First flight configuration Block II Controller (F31) shipped in place to Honeywell

April 10, 1990
Block II Controller F34 successfully hotfired at J.C.Stennis Space Center (SSC) for 265 seconds duration utilizing single DCU software

December 12, 1990
Block II Controller F40 successfully hotfired at SSC for 530 seconds duration utilizing dual DCU software (AAB08)

September 23, 1991
Block II Controllers F32 and F35 successfully completed hardware hotfire certification

November 1, 1991
Block II Controller began software hotfire certification utilizing flight software (AAA02)

March 13, 1992
Flight Readiness Firing (FRF) for OV-105 scheduled to be supported by Block II Controllers

April 16, 1992
Scheduled first Block II Controllers flight use on orbiter OV-105 (STS-49)

Design Guidelines for the Block II Controller

Primary Design Goals

: Design the Block II Controller to be mechanically and electrically equivalent to the Block I Controller

: Maintain existing engine control accuracy and stability

: Improve MCC Pc and LPFP Discharge Pressure measurement stability

: Maintain fail-op / fail-safe capability

: Utilize updated microelectronic parts having a minimum commercial availability forecast of 10 years

: Provide hardware selt-test to reduce the dependency on software to do the same function

: Improve processor and memory margins to allow higher order language and resident ground checkout program (no software overlays or patches)

: Increase reliability by decreasing the number of EEE parts using Class S parts where available

Secondary Design Goals

: Provisions for spare sensors / effectors which could be used on the next generation SSME

: Incorporation of FASCOS into the controller

: Production cost reduction

: Maintenance cost reduction

Physical Design Requirements

Size	: Length 24" x Width 14.5" x Height 18.3"
Weight	: 190 pounds or less
Parts	: Mechanical - MC, MS, AN or MIL
	: Electrical - 85M03928 Grade 1 Level
	: Connectors - RES1235 and 85M03928 (MIL-STD-975)
Seal	: Hermetically Sealed
Cooling	: Radiation and/or Convection Cooling
Redundancy	: Dual Redundant (Fail Operational after first failure, Fail-Safe after the second failure)

Electrical Design Requirements

Input Power	: AC - 3Ø, 115V (+5 V), 400 Hz
	: DC - +28V (±4V)
Processor	: MC68000 (8 MHz Model) in self-checking pair configuration
Memory	: 64K Words of CMOS RAM at 16 Bits per word in self-checking pair configuration
	: 2K Words of PROM at 16 Bits per word in self-checking pair configuration
Inputs	: 22 Temperature Sensors
	: 34 Pressure Sensors
	: 10 Pulse Rate Counters
	: 6 Igniter Monitors
	: 12 Hydraulic Actuator Valve RVDT Position Sensors
	: 15 Pressure Actuated Valve LVDT Position Sensors
	: 3 Serial Data Command Channels
	: 6 Vibration Sensors
Outputs	: 26 Solenoid Drivers
	: 18 Servoswitch Drivers
	: 6 Igniters Command Drivers
	: 12 Servovalve Drivers
	: 6 Vibration Telemetery Outputs
	: 2 Serial Data Recorder Outputs

Acceptance Test Environmental Requirements

Thermal	: 8 Thermal Cycles from -55±5°F to +95 ±5°F while operating
Vibration	: Axis X1 = 7.2 Grms, X2 = 7.13 Grms, X3 = 7.41 Grms ranging from 20 to 2000 Hz, 10 minutes per axis, hardmounted

Qualification Environmental Requirements

Thermal	: 55 Thermal Cycles from -55+5°F to +95 ±5°F while operating 5 Thermal Cycles from -55±5°F to +140 ±5°F in a vacuum while not operating
Vibration	: Workmanship - 10.77 Grms from 20 to 2000 Hz, 90 minutes per axis, hardmounted : Shock - 120 transient vibration pulses (composite shock), softmounted : Steady State - 27.64 Grms (X axis), 33.06 Grms (Y and Z axes) random vibration with super imposed sine wave 7.5 hours per axis, softmounted
EMI	: Following tests per MIL-STD-462 and SL-E-002 Conducted emission (CE01, CE03) Conducted susceptibility (CS01, CS02, CS06) Radiated emission (RE02) Radiated susceptibility (RS03) Time domain and transient ripple (TT01)
Lightning	: Meet applicable requirements of NSTS 07636 for field intensity of 150 amperes per meter
Acoustic	: 153 db near field acoustic noise for 35 minutes

Block II Qualification Test Summary

Thermal Test

55 thermal cycles from -55°F to +95°F, with 10 cold starts
Completed January 5, 1989 - TR34080203

Qualification Workmanship Vibration Test

90 minutes vibration in each axis - hardmounted
Completed January 9, 1989 - TR34080206

Steady State Vibration Test

7.5 hours vibration in each axis - softmounted
Completed January 25, 1989 - TR34080205

Transient Vibration Test

120 shocks in each axis
Completed January 25, 1989 - TR34080204

Electromagnetic Interference and Susceptibility

Conducted emission (CE01, CE03)
Conducted susceptibility (CS01, CS02, CS06)
Radiated emission (RE02)
Radiated susceptibility (RS03)
Time domain and transient ripple (TT01)
Completed March 3, 1989 - TR34080209

Acoustic Noise Test

35 minutes exposure to an acoustic noise field from 10 Hz to 10,000 Hz, with a sound level of 153 db
Completed March 23, 1989 - TR34080210

Case Ultimate Pressure Test

Pressurized to 58.9 PSIG for 2 minutes
Completed March 30, 1989 - TR34085021

Dog House and W13/14 Cable Tests

25 openings and closings of the dog house filter cover, inboard cover and electronic chassis
Completed April 3, 1989 - TR34087499

Thermal Tests (Non-operating for storage and transportation)

8 thermal vacuum cycles for -75°F to +150 °F
2 thermal cycles at ambient pressure from -55°F to +190°F with 6 hour dwells at +150°F
3 thermal cycles from -75°F to +190°F with memory hold-up voltages applied
Completed April 5, 1989 - TR34080207

Break Open Inspection

Thorough teardown hardware inspection
Completed May 8, 1989 - TR34085022

Prototype Design Verification Tests

Ground Bounce, Completed May 8, 1989 - TR34080210
Intermittent Solenoid, Completed June xx, 1989 - TR34088259
I/O Fault Insertion, Completed June xx, 1989 - TR34079282
Power Transient, TBD by HSL - TR34080202

Lightning Protection Verification Tests

Lightning Transient Analysis Completed
NSTS 07636 Rev.F deleted test, exempted SSME from Indirect Effects Verification - October 16, 1991

Block I vs Block II Controller Summary

Production Comparison

Category	Block I	Block II
Build Time	45 weeks	25 weeks
MIB - final assy time	37 weeks	11 weeks
MIB - assy method	hand solder & stitch weld	wave solder
MIB - in process assy	5,900 hours	2,700 hours
Hand solder joints	137,000	10,000
EEE Part types	1,936	840
Total Number of parts	24,479	15,806

System Comparison

Category	Block I	Block II
FASCOS	External thru DIO Bus	Internal thru IE
Special memory loader	Tape	Internal PROM
Ground checkout programs	Overlays	Resident
Failure data recorder	None	2K x 48 Bits
Weight	233 lbs with FASCOS	210 lbs
Power	620 Watts with FASCOS	400 Watts
Sensor inputs	91	106
Control outputs	44	62

Electronics Comparison

Category	Block I	Block II
Computer	Honeywell 602	Motorola 68000
Throughput	400 KIPS	573 KIPS
Error detection	Sample problem	Self-checking pair proc
Inter-DCU comm.	OE output words	Inter-DCU status register
Software language	Assembly	'C' (higher order)
Memory	16 K (Plated wire)	64K (SRAM IC's)
Access time	400 nsec read 1 usec write	75 nsec read 75 nsec write
Error detection	Parity	Self-checking data/addr
Volatility	Non-volatile	Volatile (batt backup req'd)
MIB	Stitch wire	Multi-layer circuit board

Sensor Interface Comparison

Category	Block I	Block II
I/O control	Special instructions	Memory mapped I/O
A/D conversion	10 Bit - 100 usec	12 Bit - 50 usec
Temperature Accuracy	1.5% of full scale	1.0% of full scale
Temperature Failure	Hot gas can fail qualified	Cannot fail qualified
MCC Pc / LPFP Disc Pr stability	0.50%	0.25%
IE speed	9.5 msec (all words)	6.4 msec (all words)
2 KHz source	CIEB cannot supply OEA	CIEB can supply OEA
Servoswitch monitor	Voltage	Current

Input / Output Comparison

System	Block I	Block II
Input Electronics		
Temperature sensors	20	27
Pressure sensors	32	36
Pulse rate convertors	18	10
Igniter monitors	6	6
RVDT sensors	11	12
LVDT sensors	4	15
Output Electronics		
Solenoid drivers	13	26
Servoswitch drivers	15	18
Igniters	6	6
Servovalve drivers	10	12
FASCOS		
Vibration inputs	0 (external controller)	6
Telemetry outputs	0 (external controller)	6

Card Module Comparison

Module	Block I	Block II
Input Electronics	16	11
Output Electronics	14	14
Computer Interface Electronics	15	13
Processor	14	2
Power conditioner	2	0
Memory	16	8
Voltage monitor	0	0
Totals	77	50

Engine Interface Differences

Mounting and Harness brackets differ

J14 harness required modification (connector clocked differently)

Ground straps are different lengths

Accelerometer cables are different lengths

28 VDC power (J57 on engine interface) requires capped connector to maintain Block I / Block II interchangeability on the orbiter

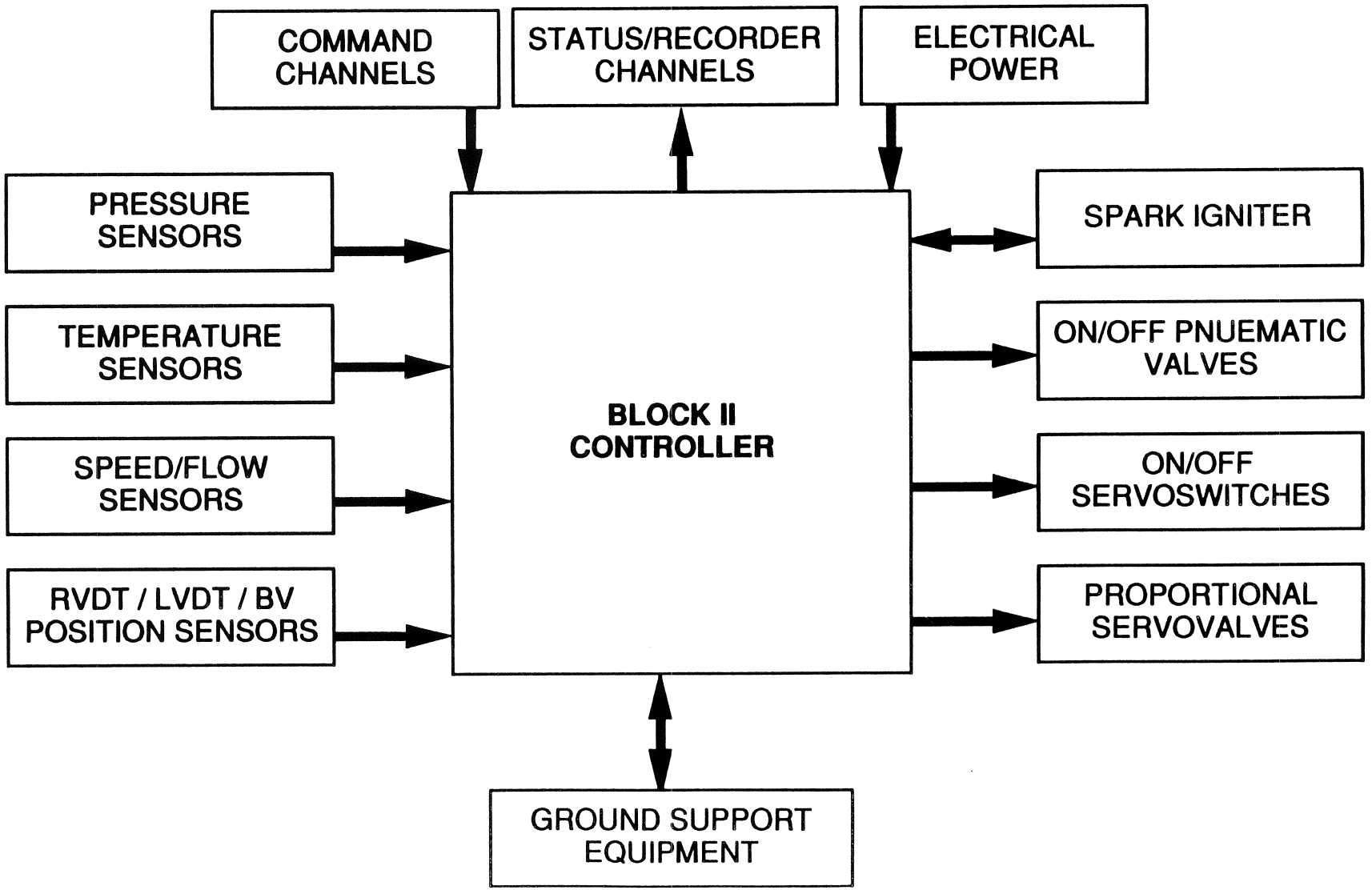
BLOCK II ELECTRONICS

EXECUTIVE OVERVIEW

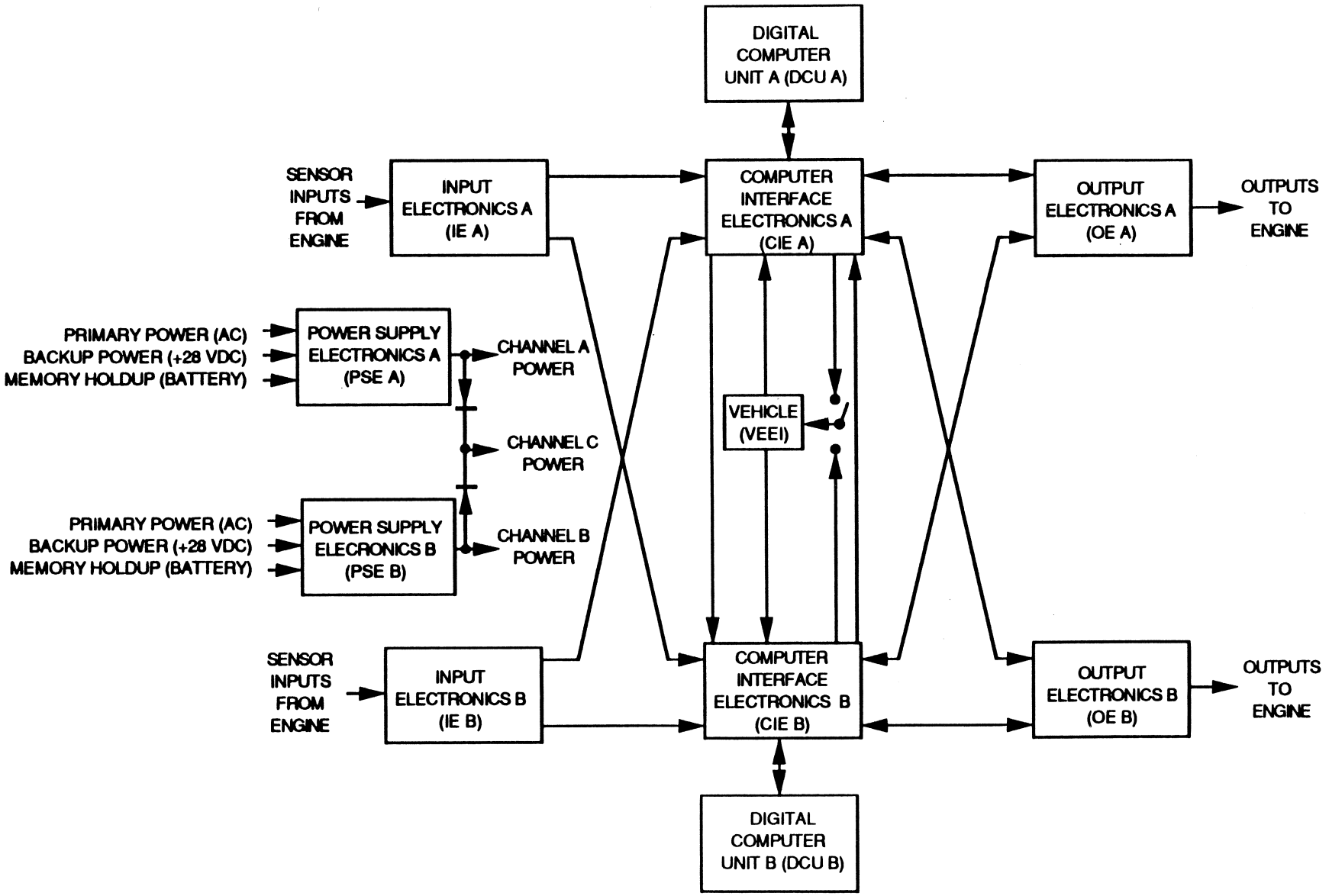
BLOCK II ELECTRONICS

- CONTROLLER INTERFACES
- CONTROLLER OVERVIEW
- INPUT ELECTRONICS (IE)
- DIGITAL COMPUTER UNIT (DCU)
- COMPUTER INTERFACE ELECTRONICS (CIE)
- OUTPUT ELECTRONICS (OE)
- POWER SUPPLY ELECTRONICS (P/S)

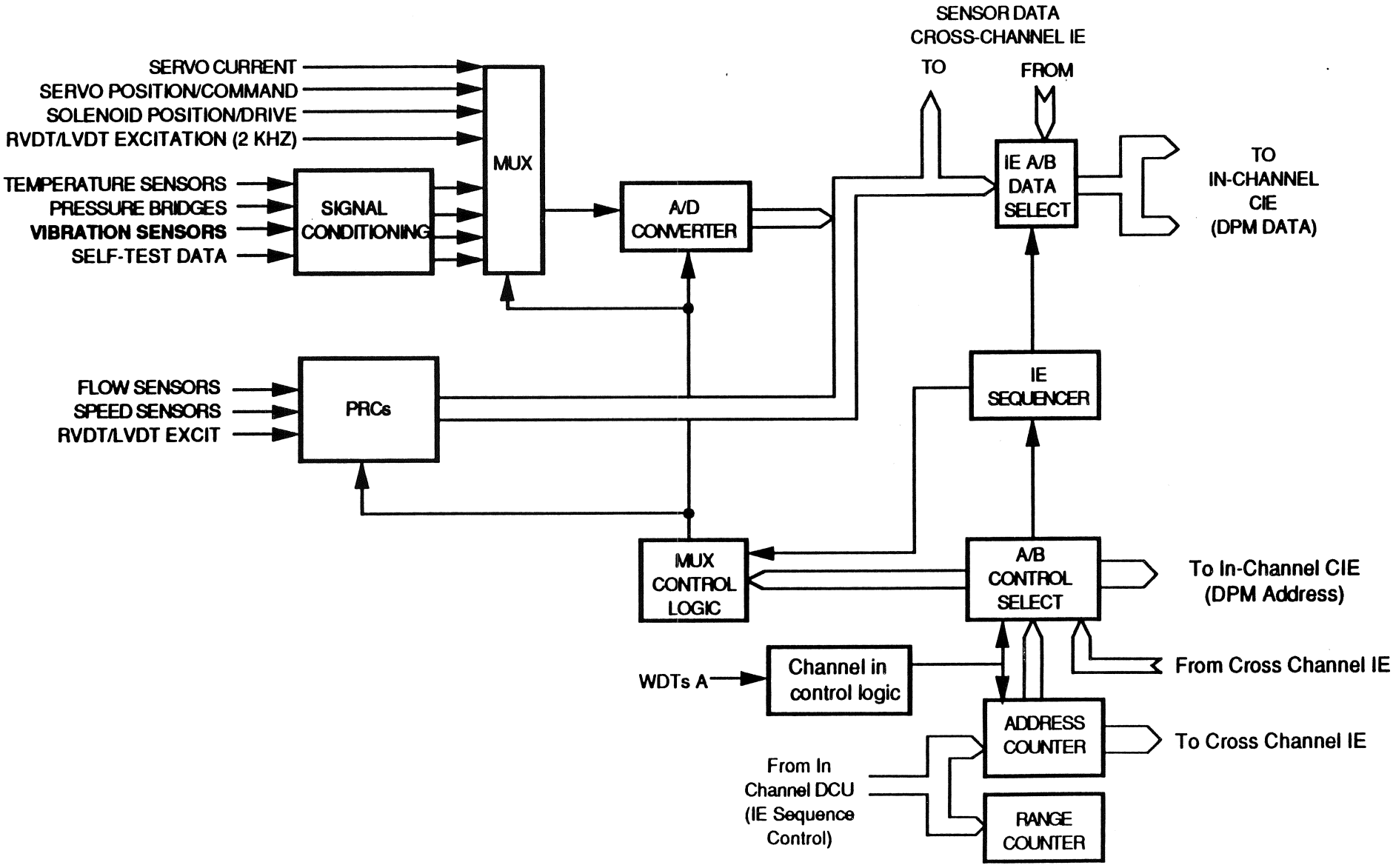
CONTROLLER INTERFACES



CONTROLLER OVERVIEW



INPUT ELECTRONICS



INPUT ELECTRONICS

FUNCTIONS:

PROVIDES SIGNAL CONDITIONING TO VARIOUS ANALOG AND PERIODIC SIGNALS

MONITORS ENGINE VIBRATION SENSORS

PROVIDES PULSE RATE COUNTING FOR PERIODIC SIGNALS

PROVIDES DIGITAL CONVERSION FOR ANALOG SIGNALS

PROVIDES SEQUENCER TO SELECT AND STORE DATA IN DUAL PORT MEMORIES

PROVIDES 500 HZ TEST SIGNAL FOR TESTING OF COUNTERS

COMPOSED OF:

SIGNAL CONDITIONERS

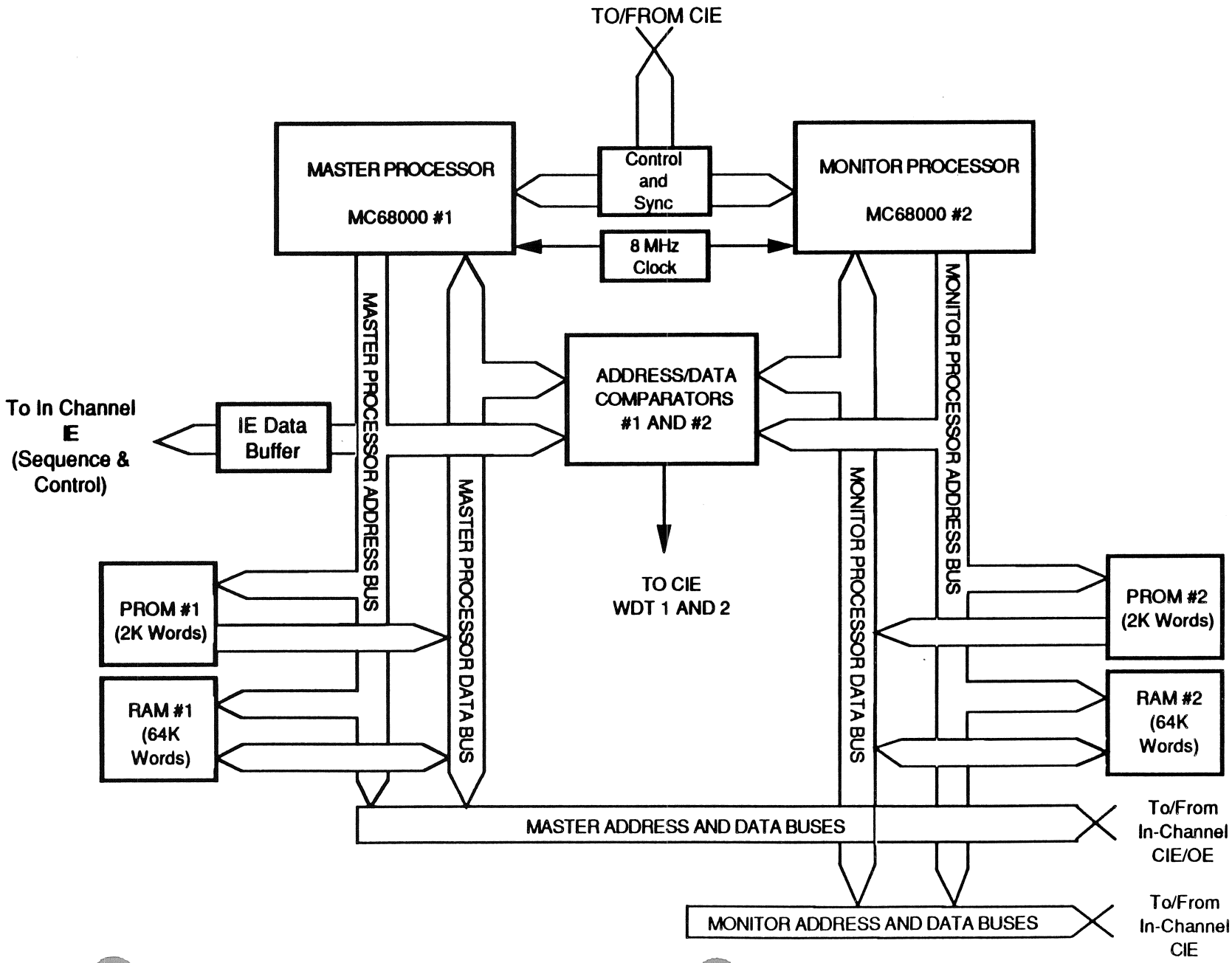
A-D CONVERTOR

PULSE RATE COUNTERS (PRCs)

IE DATA SEQUENCER

DATA SELECT CIRCUITRY

DIGITAL COMPUTER UNIT



DIGITAL COMPUTER UNIT

FUNCTIONS:

PROCESS DATA RECEIVED FROM ENGINE SENSORS

PROCESS COMMANDS RECEIVED FROM THE VEHICLE

PERFORMS ENGINE CONTROL COMPUTATIONS

PERFORMS ENGINE MONITORING COMPUTATIONS

PERFORMS ENGINE CHECKOUT COMPUTATIONS

ISSUES COMMANDS TO ENGINE CONTROL DEVICES

COMPOSED OF:

SELF-CHECKING MOTOROLA 68000 MICROPROCESSORS

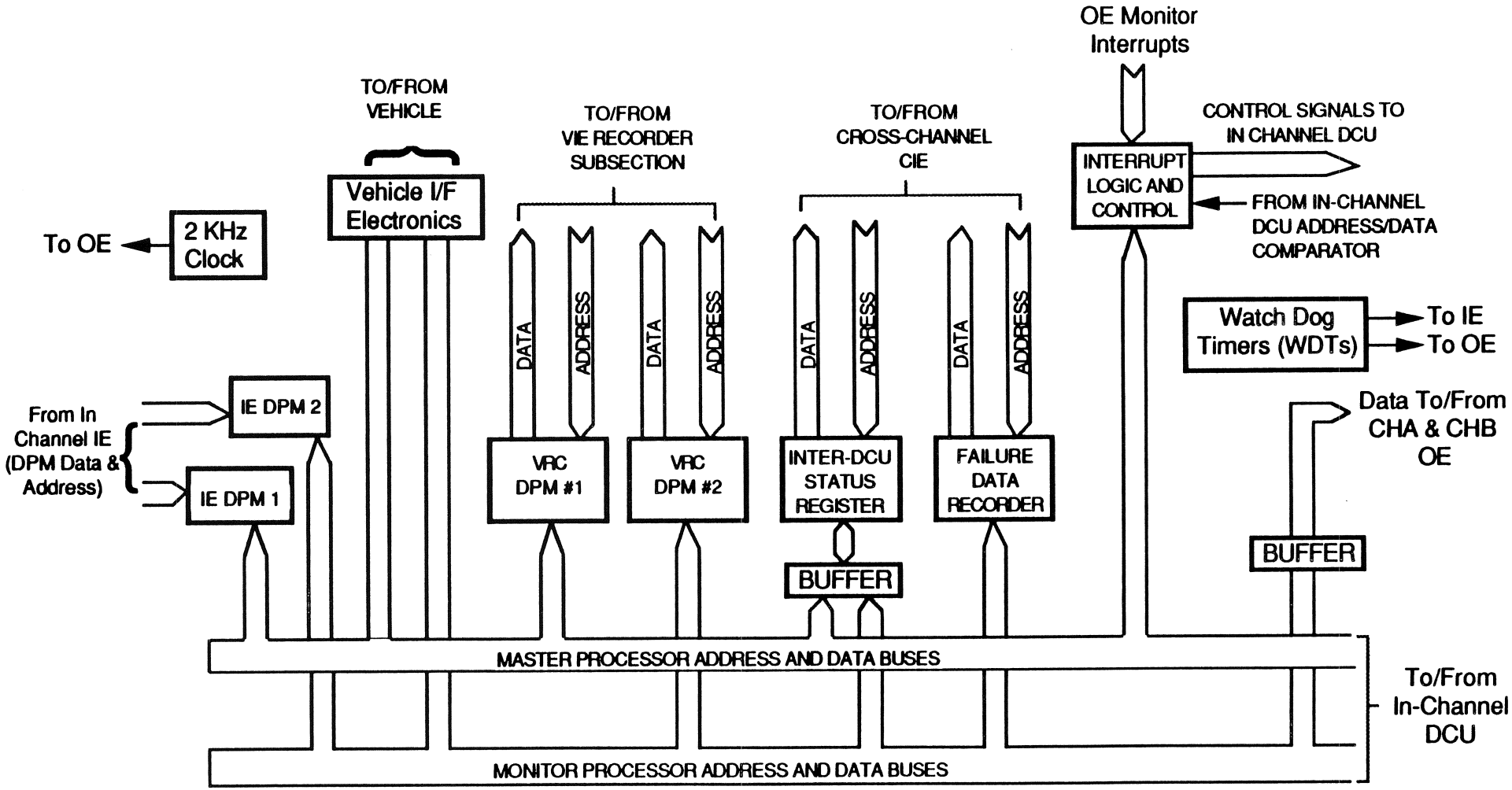
64K WORDS OF 16 BIT SRAM MEMORY FOR EACH PROCESSOR

2K WORDS OF 16 BIT PROM MEMORY PER PROCESSOR

ADDRESS AND DATA COMPARATORS

SYNCHRONIZING LOGIC

COMPUTER INTERFACE ELECTRONICS



COMPUTER INTERFACE ELECTRONICS

FUNCTIONS:

PROVIDE THE INTERFACE CIRCUITRY FOR ENGINE-CONTROLLER COMMUNICATION

PROVIDE FOR THE INTERFACE BETWEEN THE DCU AND THE IE, OE, AND CROSS-CHANNEL DCU

COMPOSED OF:

COMMAND CHANNEL DECODER

VEHICLE RECORDER DUAL PORT MEMORY (VRC DPM)

IE DUAL PORT MEMORY (IE DPM)

WATCH DOG TIMERS (WDTs)

REAL TIME COUNTER (RTC)

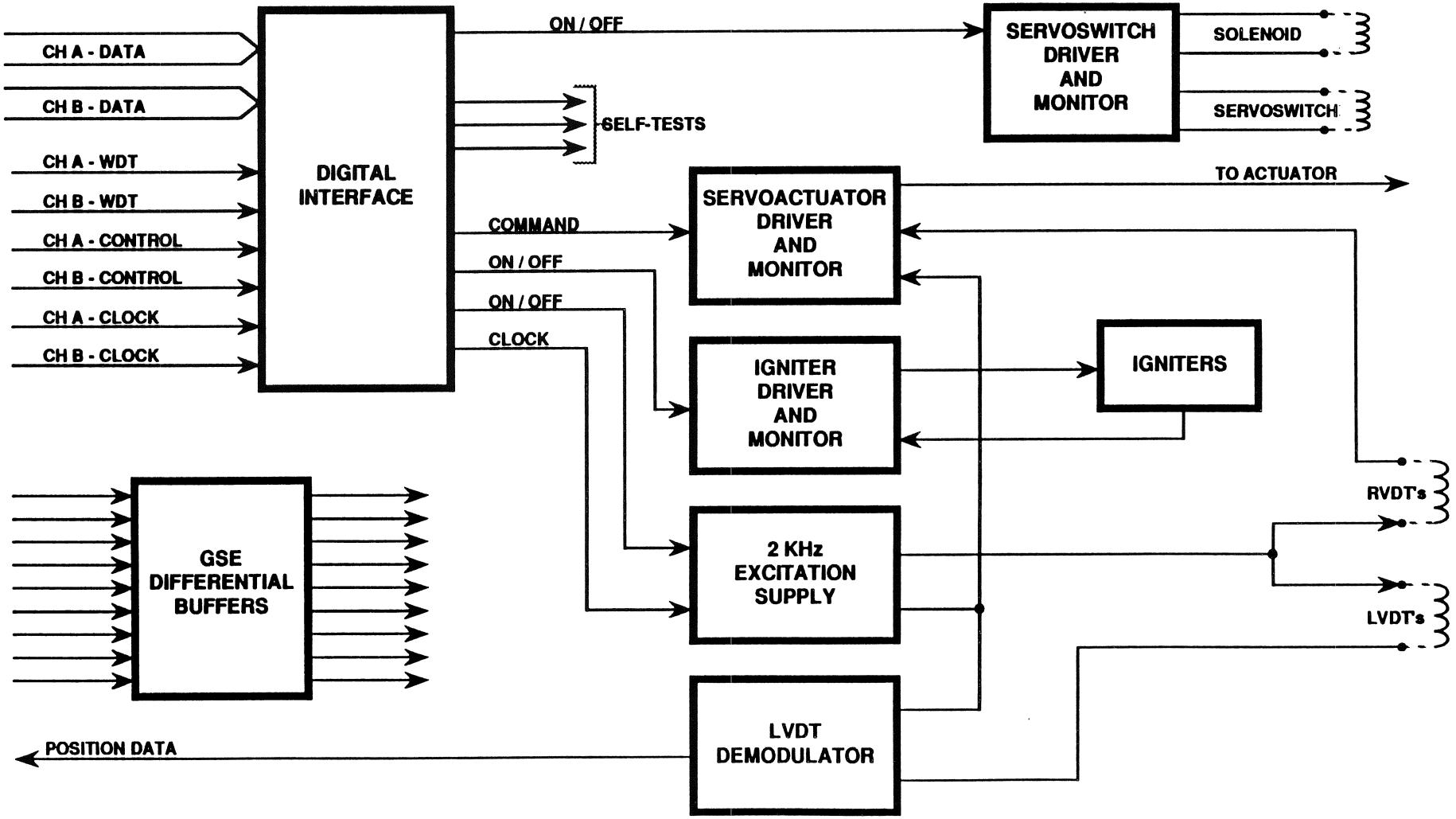
FAILURE DATA RECORDER (FDR)

INTERRUPT LOGIC AND CONTROL CIRCUITS

INTER-DCU STATUS REGISTER

MEMORY MAPPED I/O INSTRUCTION DECODE LOGIC

OUTPUT ELECTRONICS



OUTPUT ELECTRONICS

FUNCTIONS:

PROVIDES COMMAND INTERFACE BETWEEN THE DCU AND ENGINE CONTROL DEVICES

MONITORS RESPONSE OF ENGINE CONTROL DEVICES TO DCU COMMANDS THROUGH CURRENT MONITORS

MONITORS IGNITER PULSE TO VERIFY SPARKING

PROVIDES 2 KHZ EXCITATION TO RVDT'S AND LVDT'S

PROVIDES POWER OFF INDICATION OF THE 28 VDC BUS

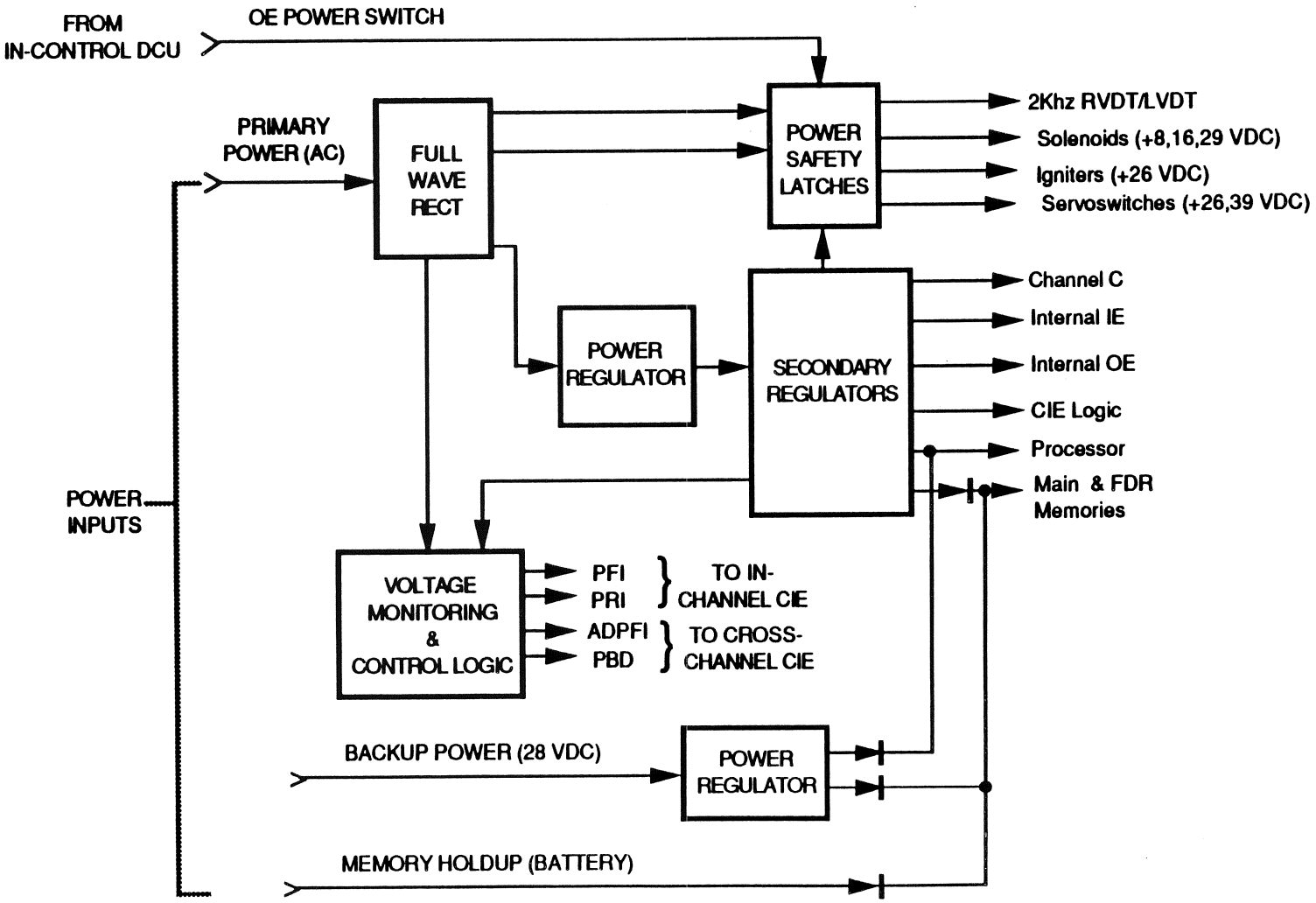
COMPOSED OF:

ON/OFF REGISTERS

EFFECTOR DRIVER / MONITOR CIRCUITRY

DIGITAL INTERFACE CIRCUITRY

POWER SUPPLY ELECTRONICS



POWER SUPPLY ELECTRONICS

FUNCTIONS:

PROVIDE CURRENT LIMITING CIRCUIT PROTECTION ON ALL OUTPUTS

PROVIDE MEMORY, FDR, AND PROCESSOR HOLD-UP FROM THE 28 VDC DURING 115 VAC FAILURE

PROVIDE MEMORY, FDR, AND PROCESSOR HOLD-UP FROM THE BATTERY DURING 115 VAC AND 28 VDC FAILURES

PROVIDE REGULATED VOLTAGES FOR USE IN THE CONTROLLER (+5, +/- 15 VDC)

PROVIDE SAFETY SWITCH VOLTAGES (+8, +16, +29, +39 VDC)

PROVIDE HOLD-UP OF REGULATED VOLATGES FOR 100 MICROSECONDS DURING POWER DOWN

PROVIDE FOR REGUALTED VOLTAGE MONITORING

COMPOSED OF:

FULL WAVE RECTIFIER

POWER REGULATORS

SECONDARY REGULATOR

VOLTAGE MONITORS

BLOCK II CONTROLLER
TECHNICAL OVERVIEW

SECTION 1 - INPUT ELECTRONICS

SECTION 2 - DIGITAL COMPUTER UNIT

SECTION 3 - COMPUTER INTERFACE ELECTRONICS

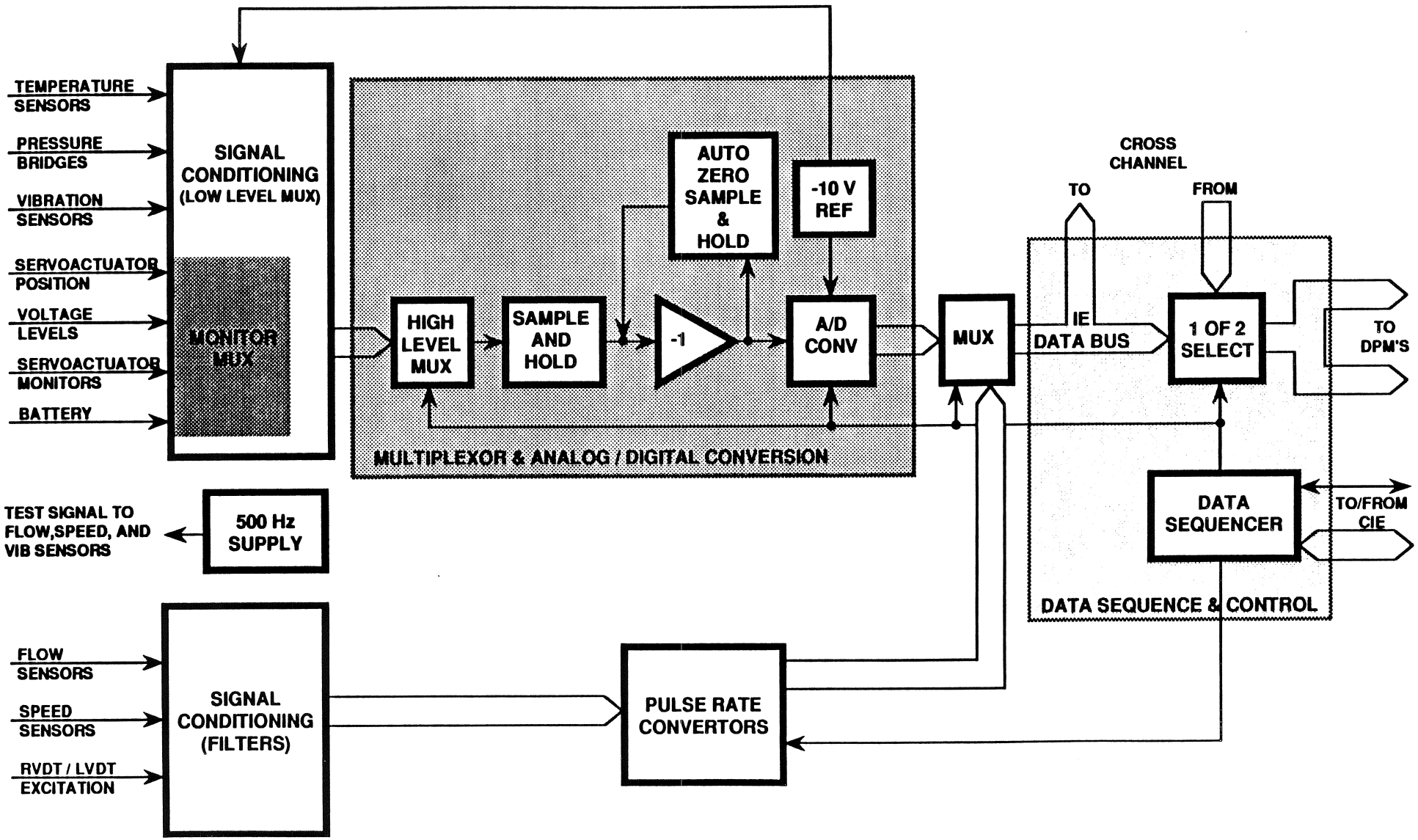
SECTION 4 - OUTPUT ELECTRONICS

SECTION 5 - POWER SUPPLY

BLOCK II INPUT ELECTRONICS (IE)
FUNCTIONS

- PROVIDES SIGNAL CONDITIONING FOR VARIOUS ANALOG SENSORS
  - 27 TEMP SENSORS
  - 36 PRESSURE SENSORS
- MONITORS SIX ENGINE VIBRATION SENSORS
- PROVIDES FILTERS & PULSE RATE COUNTERS FOR PERIODIC SIGNALS
  - 4 FLOW SENSORS
  - 6 SPEED SENSORS
  - RVDT/LVDT EXCITATION
- MONITORS EFFECTOR RESPONSE THROUGH MONITOR MUX
  - RVDT POSITION
  - SERVOACTUATOR CURRENT MONITORS
- MONITORS INTERNAL VOLTAGE LEVELS THROUGH MONITOR MUX
- PROVIDES SEQUENCER LOGIC TO SELECT AND STORE DATA INTO DUAL PORT MEMORIES
- PROVIDES 500 Hz TEST SIGNAL FOR TESTING OF PERIODIC COUNTERS

INPUT ELECTRONICS



BLOCK II INPUT ELECTRONICS
FUNCTIONAL BLOCKS

- THE BLOCK II CONTROLLER INPUT ELECTRONICS IS DIVIDED INTO THE FOLLOWING FUNCTIONAL BLOCKS
  - SIGNAL CONDITIONING (LOW LEVEL AND MONITOR MUXES)
    - PROVIDES FOR TEMPERATURE AND PRESSURE BRIDGE COMPLETION
    - CONTAINS LOW-LEVEL ANALOG MUX
    - CONTAINS THE MONITOR MUX
    - SUPPORTS PROP-DROP MODE
    - CONTAINS SELF-TEST LOGIC
    - PROVIDES FOR SENSOR CALIBRATION
  - MULTIPLEXOR AND A/D CONVERSION
    - PROVIDE FOR HIGH LEVEL MUXING OF INPUT DATA
    - PROVIDE FOR ANALOG TO DIGITAL CONVERSION OF INPUT DATA

BLOCK II INPUT ELECTRONICS
FUNCTIONAL BLOCKS

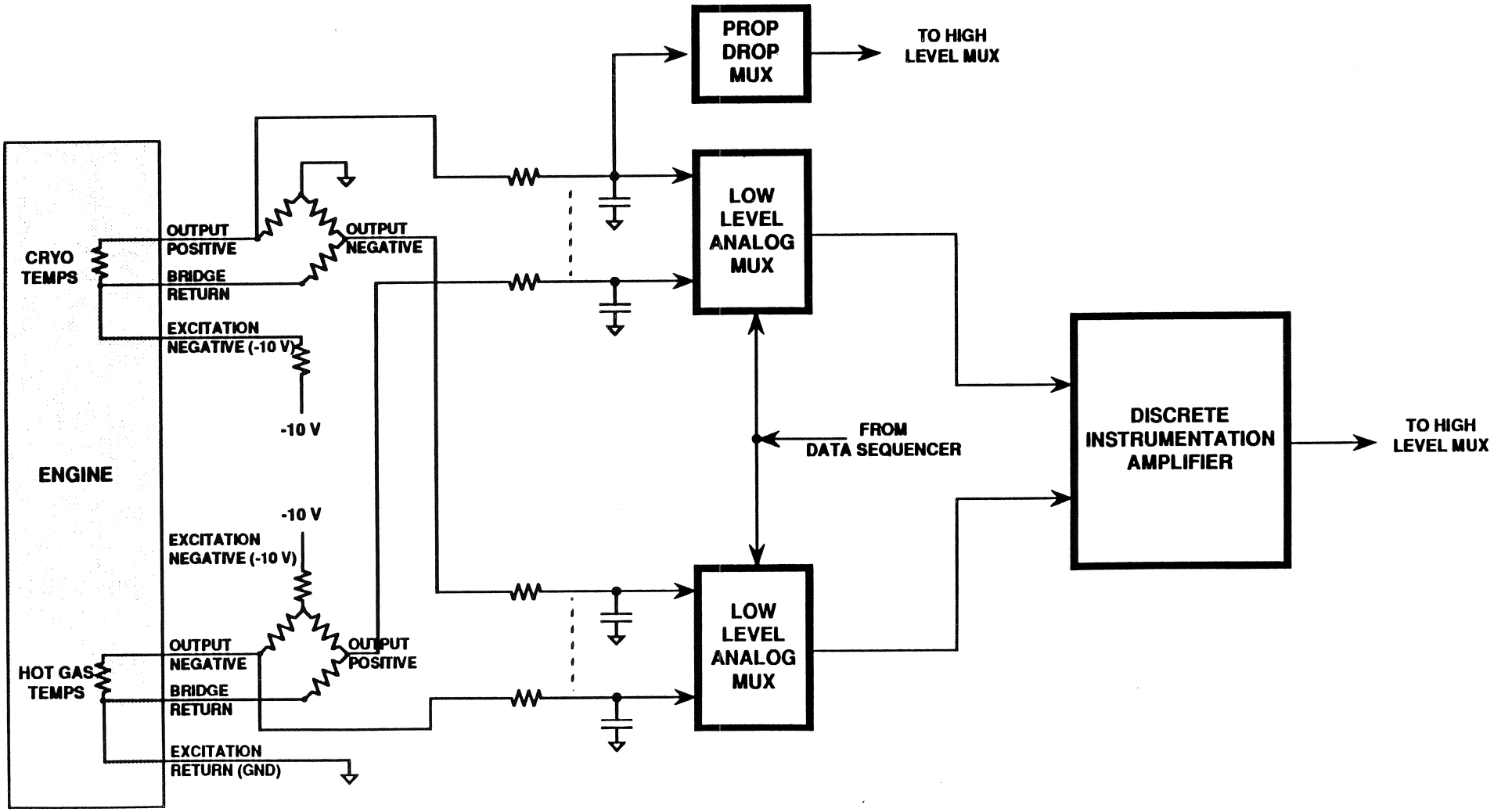
- 500 Hz SUPPLY
    - PROVIDES FOR 500 Hz TEST SIGNAL FOR PERIODIC INPUTS
- PULSE RATE COUNTERS
    - PROVIDES FOR CONVERSION OF PERIODIC SIGNALS
    - OUTPUT REPRESENTS PULSE INTERVAL MEASUREMENT
- IE DATA SEQUENCER
    - PROVIDES THE SEQUENCING LOGIC TO CONTROL MUXING AND A/D CONVERSION
    - CONTROLS THE IE DUAL PORT MEMORY (DPM)

BLOCK II INPUT ELECTRONICS
FUNCTIONS BY CARD

- THE BLOCK II IE CONSISTS OF SIX CARDS

FUNCTIONS	MODULE
TEMPERATURE SIGNAL CONDITIONING	IE1
PRESSURE SIGNAL CONDITIONING	IE2
ANALOG TO DIGITAL CONVERSION	IE2
PULSE RATE COUNTERS (FLOW)	IE3
500 Hz SUPPLY	IE3
PULSE RATE COUNTERS (SPEED)	IE4
CROSS CHANNEL DATA MUX	IE4
SEQUENCING LOGIC	IE5
VSPE HYBRIDS (CHANNEL A ONLY)	IE6

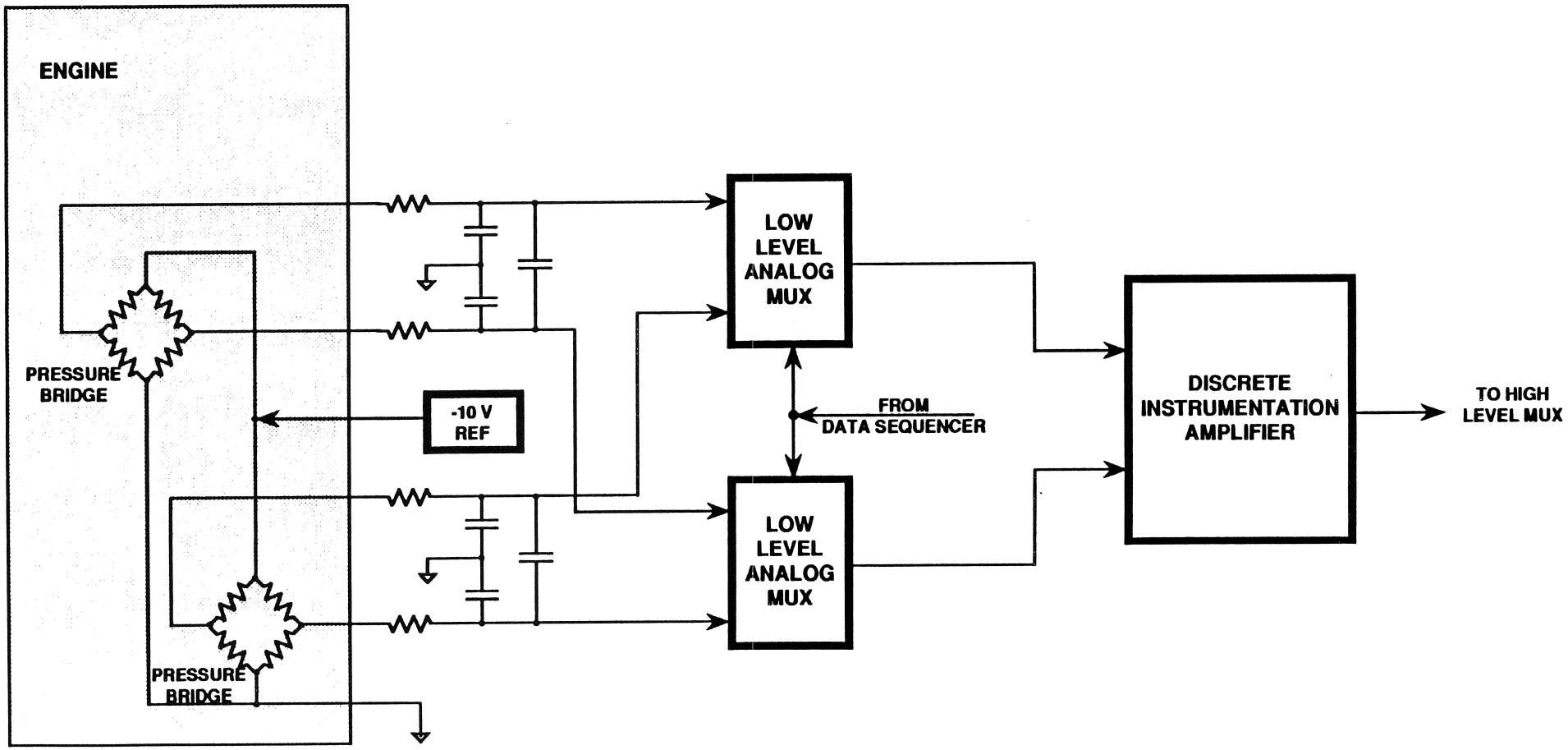
INPUT ELECTRONICS
TEMPERATURE SIGNAL PROCESSING



BLOCK II INPUT ELECTRONICS
SIGNAL CONDITIONING - TEMPERATURE

- TEMPERATURE BRIDGES
  - HOT GAS
  - CRYOGENIC
- LOW LEVEL ANALOG MUX
  - A 24 TO 1 DIFFERENTIAL MUX WHICH IS DIVIDED INTO THREE GROUPS OF EIGHT
- DISCRETE INSTRUMENTATION AMPLIFIER
  - DIFFERENTIAL AMPLIFIER WITH A GAIN OF 25.83 V/V
- PROVIDES FOR 50% CALIBRATION SWITCHES

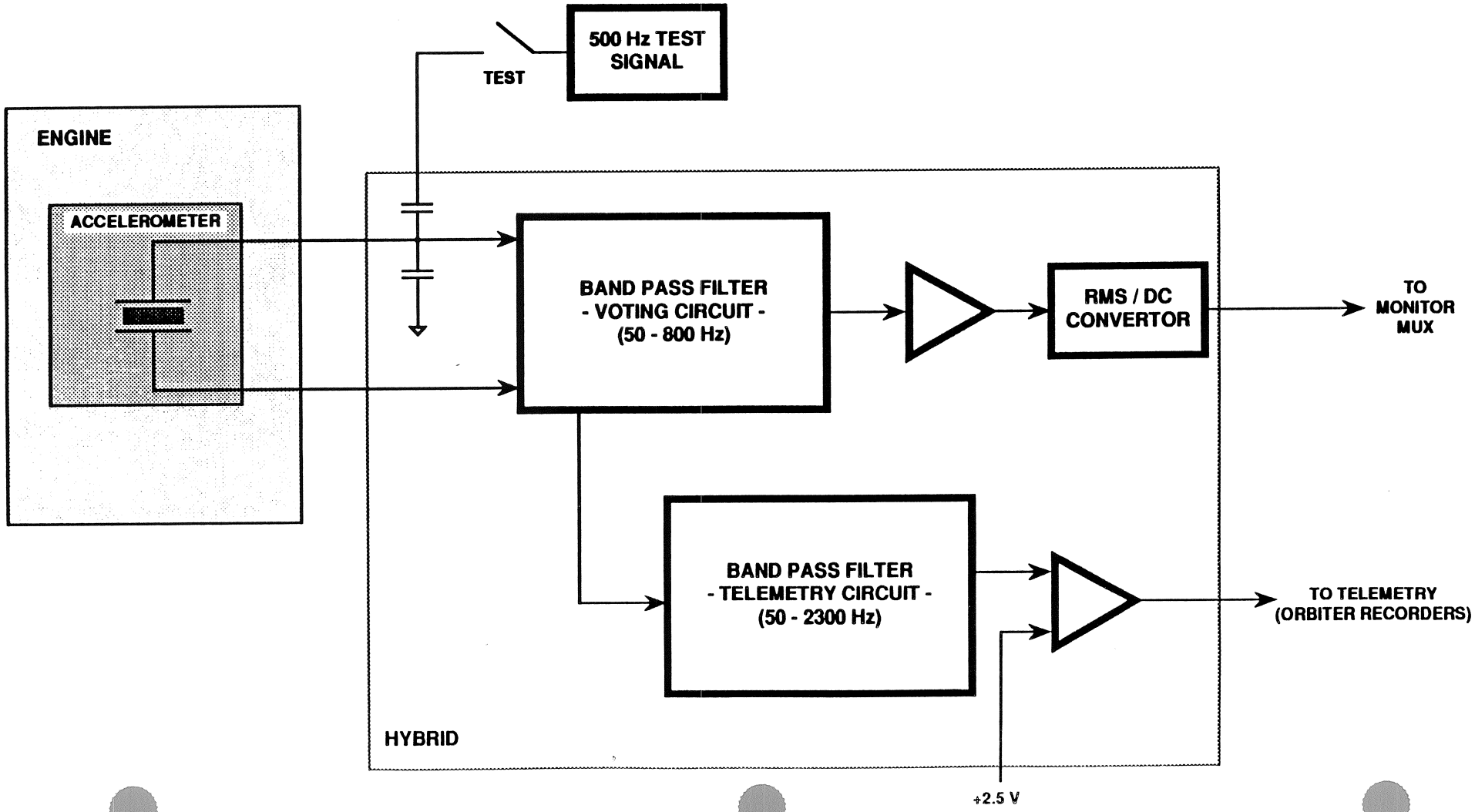
INPUT ELECTRONICS
PRESSURE SIGNAL PROCESSING



BLOCK II INPUT ELECTRONICS
SIGNAL CONDITIONING - PRESSURE

- PRESSURE INPUT
  - OUTPUT OF PRESSURE SENSORS IS ROUTED THROUGH A LOW-PASS ANTI-ALIASING FILTER
  - 0 TO 30 mV INPUT FROM EXTERNAL BRIDGES
  - PROVIDES FOR 80% CALIBRATION SWITCHES
- LOW LEVEL ANALOG MUX
  - A 32 TO 1 DIFFERENTIAL MUX WHICH IS DIVIDED INTO FOUR GROUPS OF EIGHT
- DISCRETE INSTRUMENTATION AMPLIFIER
  - DIFFERENTIAL AMPLIFIER WITH A GAIN OF 150.33 V/V

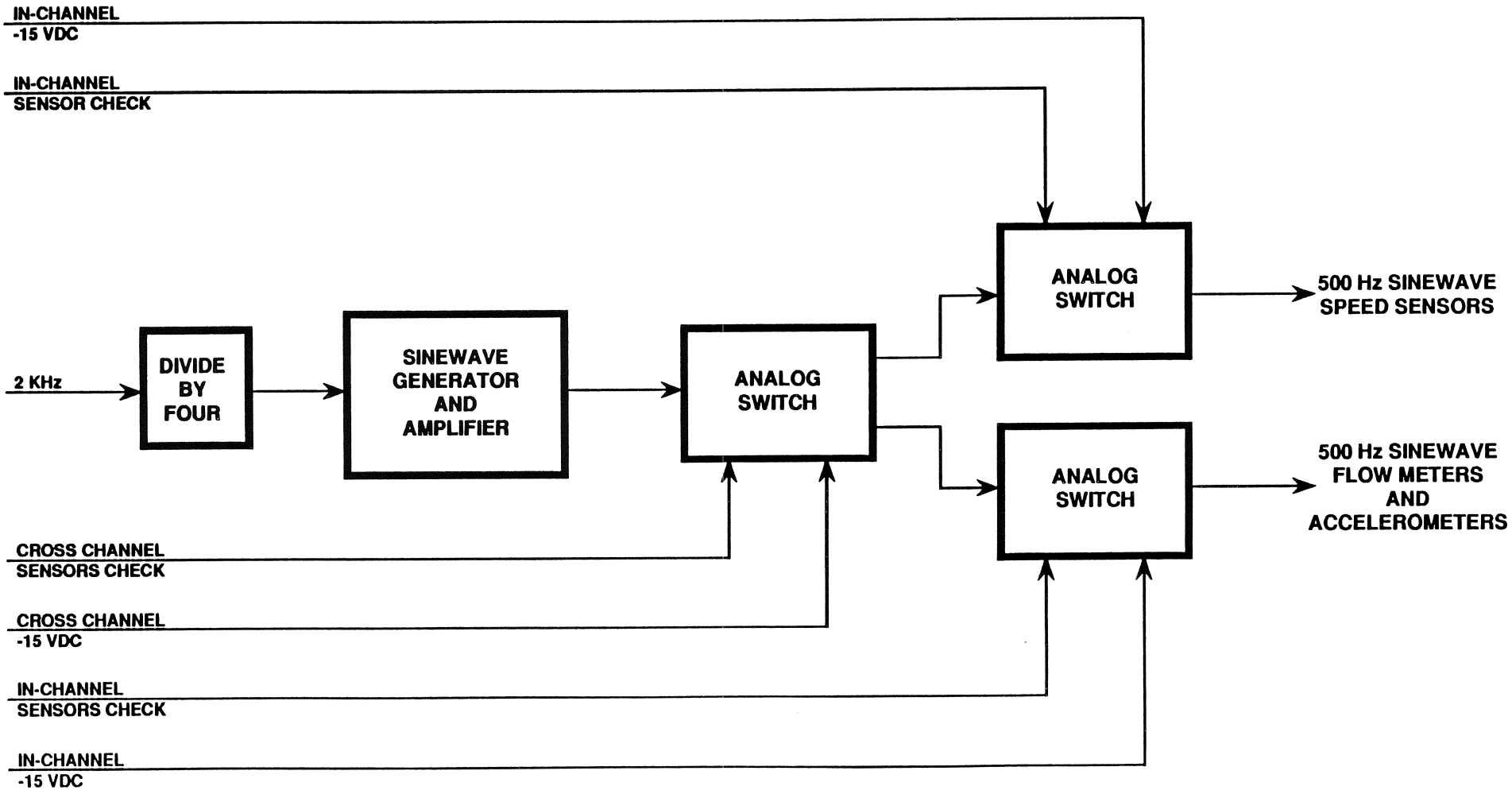
INPUT ELECTRONICS
VIBRATION SIGNAL PROCESSING



BLOCK II INPUT ELECTRONICS
VIBRATION SIGNAL PROCESSING

- VSPE HYBRIDS
  - VOTING CIRCUIT
    - PROVIDE FOR BAND PASS FILTERING OF VIBRATION SIGNALS
      - 50 - 800 Hz
    - FILTERED OUTPUT IF PROCESSED THROUGH THE RMS/DC CONVERTER
    - OUTPUT IS SENT TO THE MONITOR MUX
  - TELEMETRY CIRCUIT
    - PROVIDE FOR BAND PASS FILTERING OF VIBRATION SIGNALS
      - 50 - 2300 Hz (OFFSET BY 2.5 VOLTS)

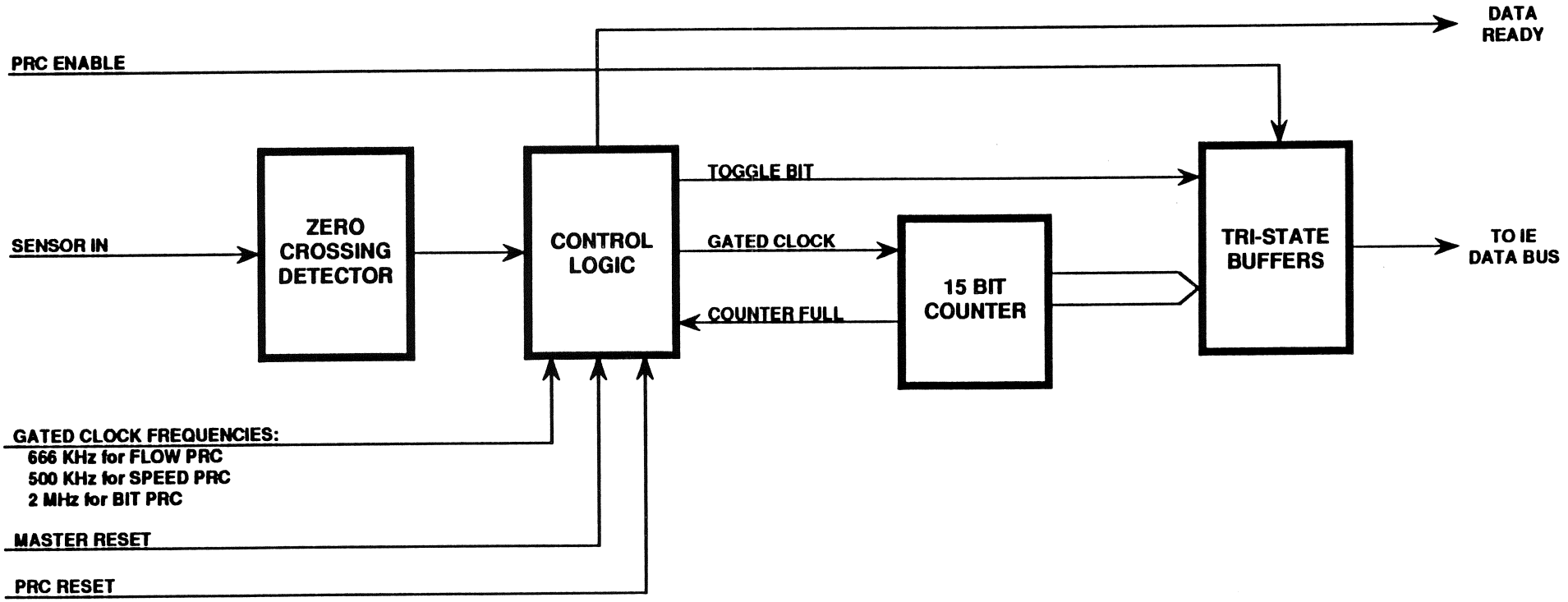
INPUT ELECTRONICS
500 Hz SUPPLY



BLOCK II INPUT ELECTRONICS
500 Hz SUPPLY

- SINEWAVE GENERATOR AND AMPLIFIER
  - RECEIVES THE 2 KHz SQUARE WAVE AS INPUT
  - DIVIDES THE SQUARE WAVE BY FOUR
  - SHAPES THE 500 Hz SQUARE WAVE INTO A 1.22 Vrms SINE WAVE
- ANALOG SWITCH
  - REDUNDANT SWITCHES THAT ARE CONTROLLED BY EACH CHANNEL
  - PROVIDE TEST SIGNALS FOR PRCs AND VSPE

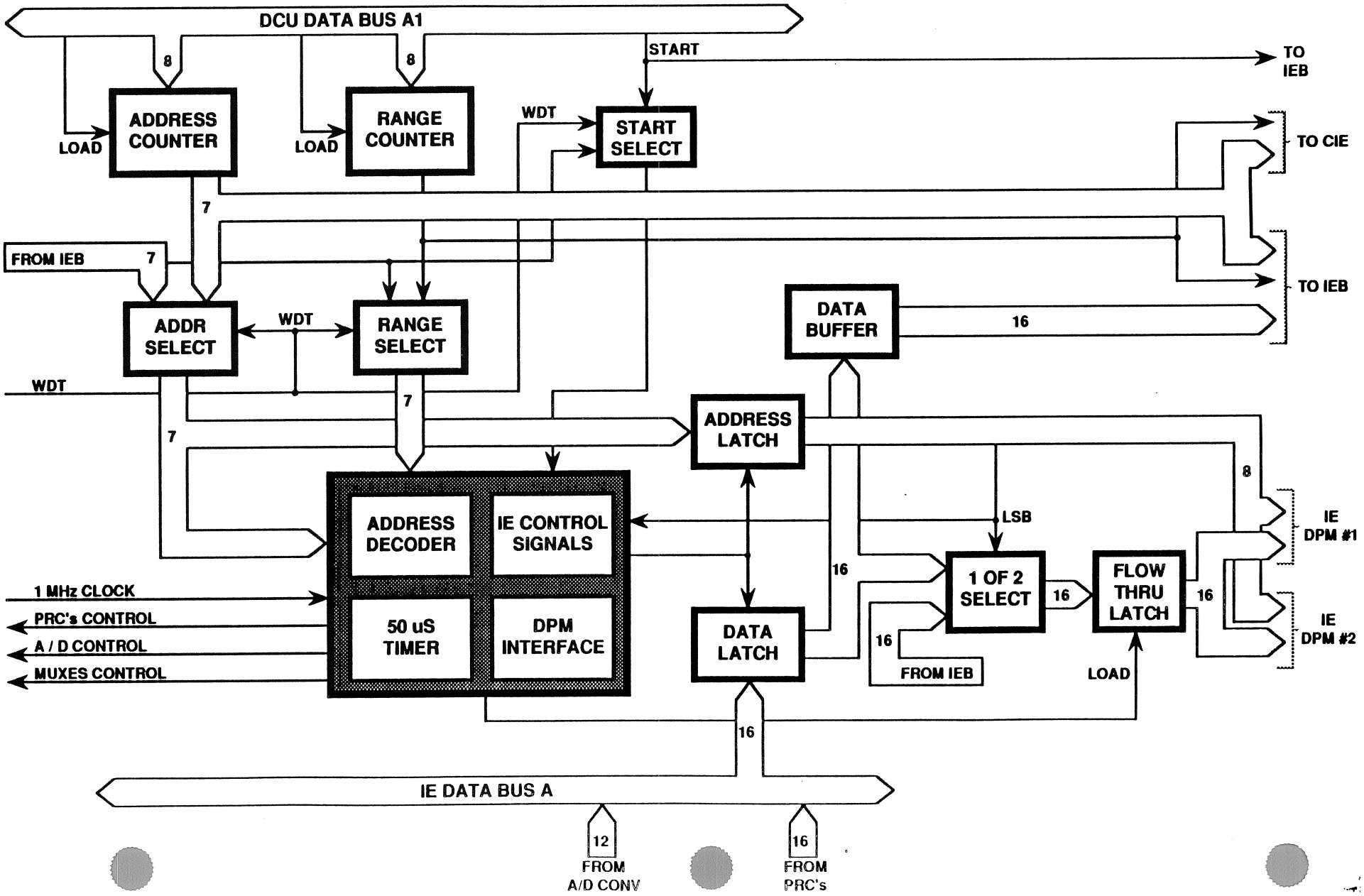
INPUT ELECTRONICS
PULSE RATE COUNTER (PRC)



BLOCK II INPUT ELECTRONICS
PULSE RATE COUNTERS

- ZERO CROSSING DETECTOR
  - DETECTS WHEN INPUT VALUE CROSSES 0 VOLTS
- CONTROL LOGIC / 15 BIT COUNTER
  - COUNT THE NUMBER OF PULSES FROM THE GATED CLOCK FREQUENCIES BETWEEN ZERO CROSSING'S
  - SIGNAL THAT THE DATA IS READY FOR OUTPUT TO THE IE DPM
  - TOGGLE BIT INDICATES DATA UPDATE

INPUT ELECTRONICS
DATA SEQUENCER



BLOCK II INPUT ELECTRONICS
IE DATA SEQUENCER

- SEQUENCE INITIATION (START SELECT)
    - ALLOWS THE IN-CONTROL CHANNEL TO INITIATE IE PROCESSING ON BOTH IE's
- ADDRESS COUNTER
    - CONTAINS THE START ADDRESS OF THE FIRST IE DATA PAIR TO BE PROCESSED
- RANGE COUNTER
    - CONTAINS THE NUMBER OF IE DATA PAIRS TO BE PROCESSED
    - DECREMENTED BY ONE AFTER EACH PAIR IS PROCESSED
- ADDRESS SELECT
    - SELECTS THE ADDRESS COUNTER FROM THE IN-CONTROL CHANNEL BASED UPON THE STATUS OF THE WDT's
- RANGE SELECT
    - SELECTS THE RANGE COUNTER FROM THE IN-CONTROL CHANNEL BASED UPON THE STATUS OF THE WDT's

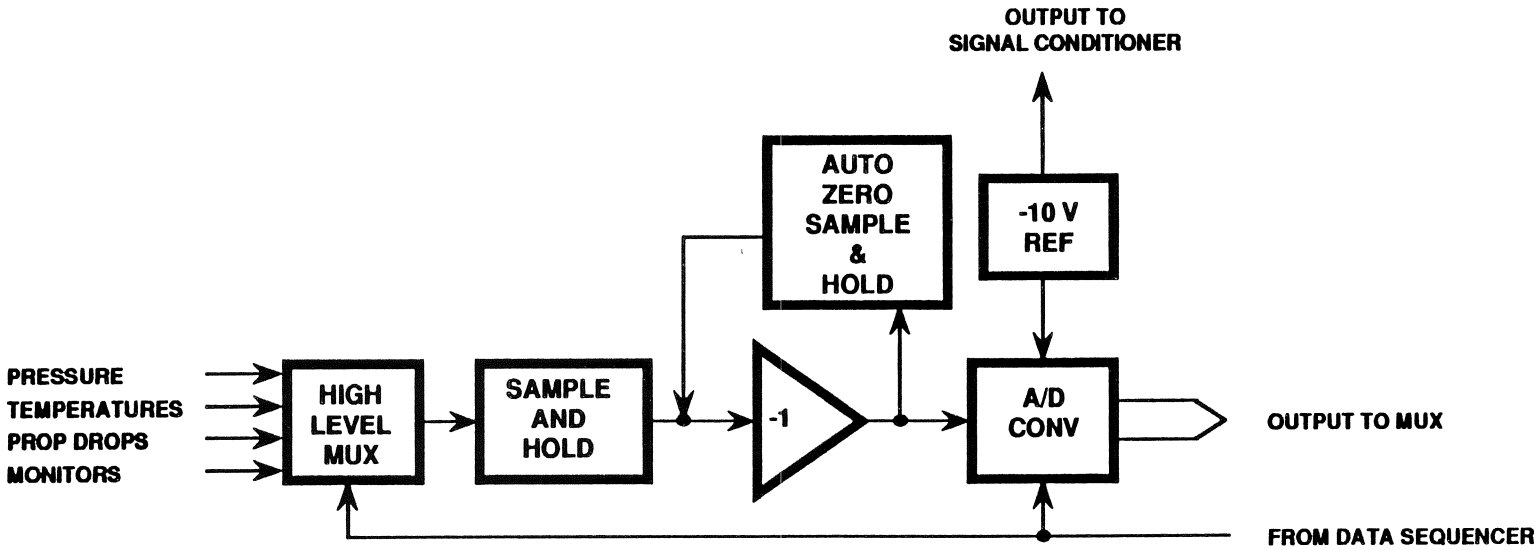
BLOCK II INPUT ELECTRONICS
IE DATA SEQUENCER

- ADDRESS DECODER
  - CREATES GROUP / TEST ENABLE SIGNALS BASED ON ADDRESS
    - GROUP 1 THRU 7 ARE THE ENABLES TO THE MONITOR MUX's
    - GROUP 8 THRU 10 ARE THE ENABLES TO THE TEMPERATURE MUX's
    - GROUP 11 ENABLES PRCs
    - GROUP 12 THRU 15 ARE THE ENABLES TO THE PRESSURE MUX's
- 50 uS TIMER
  - DERIVED FROM 1 MHz CLOCK
  - CONTROLS TIMING OF IE DATA PAIR PROCESSING (1 PAIR EVERY 50 us)
- IE CONTROL SIGNALS
  - GENERATES CONTROL SIGNALS FOR A/D CONVERSION, PRC ENABLE, DPM REQUESTS AND RANGE COUNTER DECREMENTATION
- DPM INTERFACE
  - CONTROLS THE LOAD OF DATA INTO THE DPM

BLOCK II INPUT ELECTRONICS
IE DATA SEQUENCER

- ADDRESS LATCH
  - PROVIDES SYNCHRONOUS CONTROL OF ADDRESSING TO DPM's
- DATA LATCH
  - PROVIDES SYNCHRONOUS CONTROL OF DATA TO DPM's
- 1 0F 2 SELECT
  - SELECTS DESTINATION DPM BASED UPON ADDRESS LSB

INPUT ELECTRONICS
ANALOG TO DIGITAL CONVERSION



BLOCK II INPUT ELECTRONICS
ANALOG TO DIGITAL CONVERSION

- HIGH LEVEL MUX
    - SELECTS EITHER THE TEMPERATURE, PRESSURE, PROP DROP T TEMPERATURES OR THE MONITOR MUX OUTPUTS FOR A/D CONVERSION
    - CONTROLLED BY IE SEQUENCER LOGIC
- SAMPLE AND HOLD CIRCUITS
    - CONTINUOSLY SAMPLES THE OUTPUT OF THE HIGH LEVEL MUX
    - HOLDS THE OUTPUT OF THE MUX DURING A CONVERSION
- AUTO ZERO SAMPLE AND HOLD
    - THIS CIRCUIT IS ACTIVE AFTER READING THE FIRST MEASUREMENT IN GROUP 9 OR GROUP 12 (THIS IS A GROUND VALUE)
    - THE CIRCUIT THEN FEEDS THE INVERSE OF THE GROUND VALUE INTO THE A/D TO ELIMINATE ANY OFFSETS IN THE SYSTEM
- ANALOG TO DIGITAL CONVERSION
    - 12-BIT A/D CONVERTOR WITH A RANGE OF ±5 VDC
    - OUTPUT IS IN 2'S COMPLEMENT

BLOCK II CONTROLLER
TECHNICAL OVERVIEW

SECTION 1 - INPUT ELECTRONICS

SECTION 2 - DIGITAL COMPUTER UNIT

SECTION 3 - COMPUTER INTERFACE ELECTRONICS

SECTION 4 - OUTPUT ELECTRONICS

SECTION 5 - POWER SUPPLY

BLOCK II DIGITAL COMPUTER UNIT (DCU)
FUNCTIONS

- PROCESS DATA RECEIVED FROM ENGINE SENSORS
- PROCESS COMMANDS RECEIVED FROM THE VEHICLE
- PERFORM ENGINE CONTROL COMPUTATIONS
    - MIXTURE RATIO (FPOV CLOSED LOOP CONTROL)
    - THRUST CONTROL (OPOV CLOSED LOOP CONTROL)
- PERFORMS ENGINE MONITORING COMPUTATIONS
- PERFORMS ENGINE CHECKOUT COMPUTATIONS
- ISSUE COMMANDS TO ENGINE CONTROL DEVICES
- CONTROLS VEHICLE DATA TABLE TRANSFER TO ORBITER

BLOCK II DIGITAL COMPUTER UNIT
FUNCTIONAL BLOCKS

- THE BLOCK II CONTROLLER DCU IS DIVIDED INTO THE FOLLOWING FUNCTIONAL BLOCKS
  - SELF-CHECKING PAIR PROCESSORS (SCP's)
    - DUAL LOOSELY COUPLED MC68000 MICROPROCESSORS
    - DUAL DATA AND ADDRESS COMPARATORS
    - INITIALIZATION PROGRAMMABLE READ ONLY MEMORY (PROM)
  - MAIN PROGRAM MEMORY
    - DUAL 64K STATIC RANDOM ACCESS MEMORY (SRAM)
      - DIVIDED INTO TWO GROUPS - UPPER 32K AND LOWER 32K
    - NO 'WAIT STATES' FOR READ/WRITE ACCESS
    - REQUIRES POWER TRANSIENT PROTECTION FOR VOLATILE MEMORY

BLOCK II DIGITAL COMPUTER UNIT
FUNCTIONS BY CARD

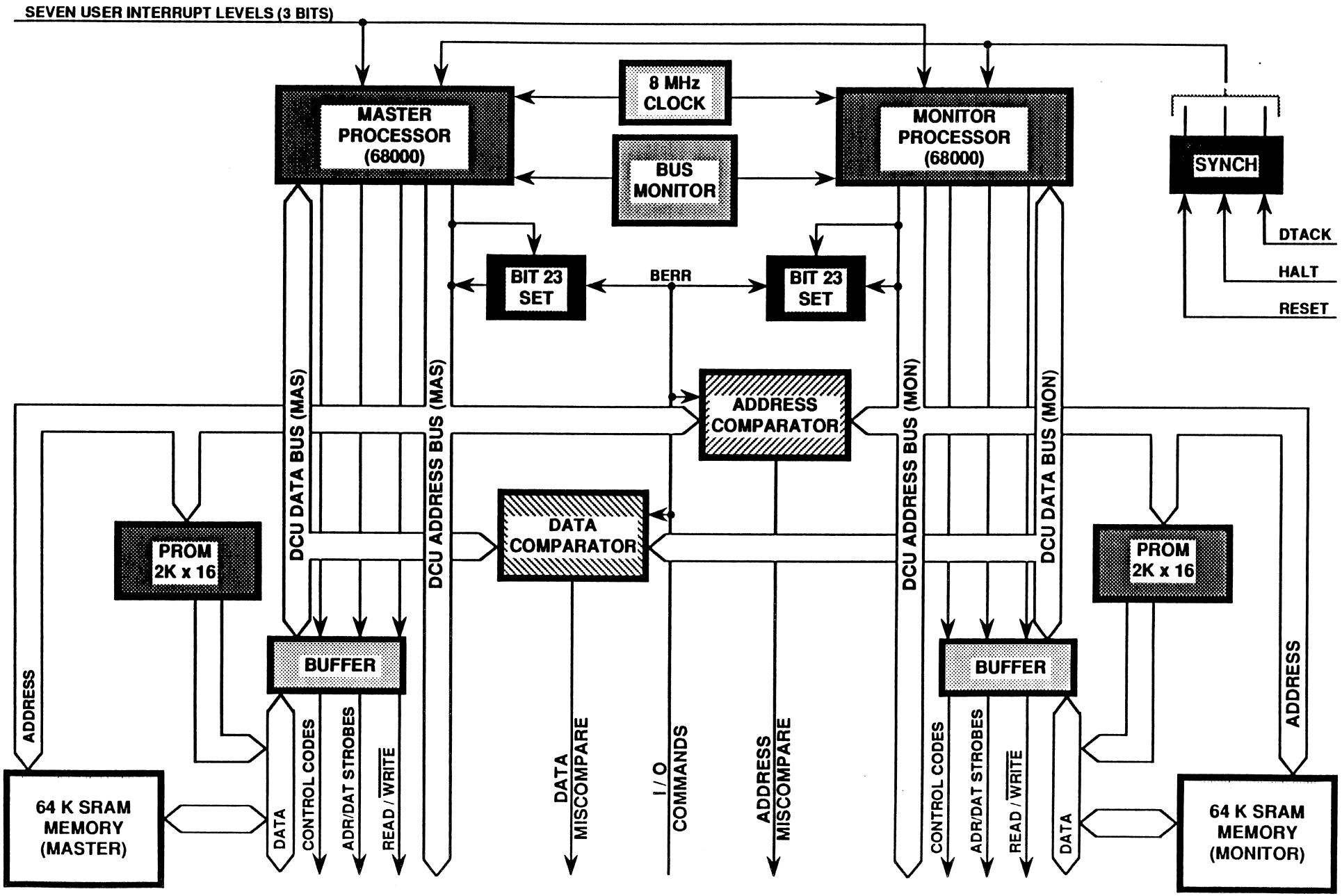
- THE BLOCK II DCU CONSISTS OF SIX CARDS

FUNCTIONS	MODULE
SELF-CHECKING PAIR PROCESSORS	PROC
MEMORY INTERFACE	MEM IF
32K LOWER MEMORY (MASTER)	A9/A10
32K UPPER MEMORY (MASTER)	A13/A14
32K LOWER MEMORY (MONITOR)	A36/A37
32K UPPER MEMORY (MONITOR)	A40/A41

DCU ADDRESS SPACE

WORDS	EVEN BYTE		ODD BYTE	BYTES
	FFFFFE		FFFFFF	
32,768		SRAM		65,536
	FF0000		FF0001	
	FEFFFE		FEFFFF	
4,093,952		UNUSED		8,187,904
	821000		821001	
	820FFE		820FFF	
2,048	820000	INPUT / OUTPUT	820001	4,096
	81FFFE		81FFFF	
63,488		UNUSED		126,976
	801000		801001	
	80FFE		80FFF	
2,048	800000	PROM	800001	4,096
	7FFFFE		7FFFFF	
4,161,536		UNUSED		8,323,072
	010000		010001	
	00FFFE		00FFFF	
32,768		SRAM (VECTORS)		65,536
	000000		000001	

DIGITAL COMPUTER UNIT



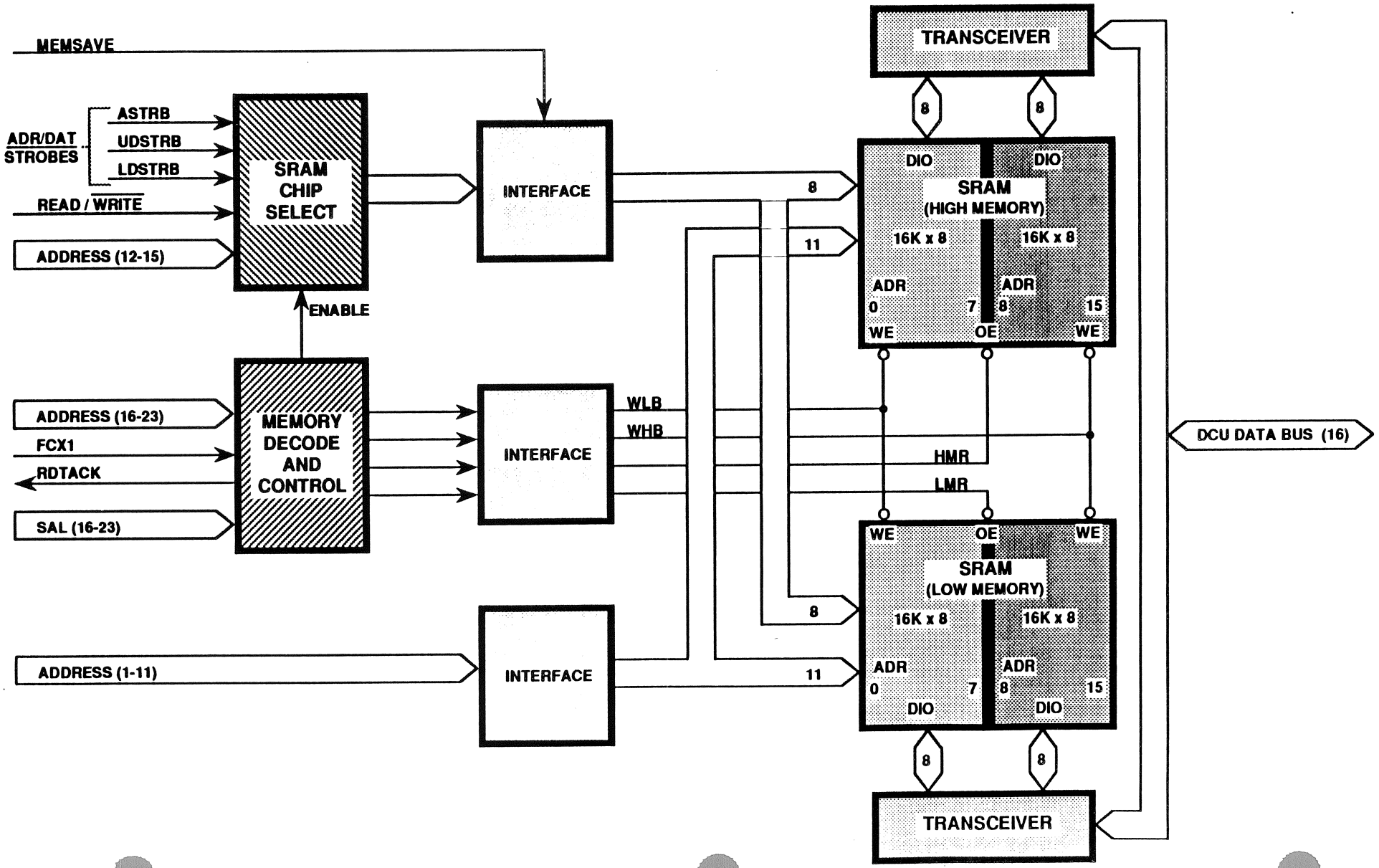
BLOCK II DIGITAL COMPUTER UNIT
SELF-CHECKING PAIR PROCESSOR

- MOTOROLA 68000
  - 8 MHz, 16 BIT PROCESSOR
  - 23 BIT ADDRESS FIELD
- BUS MONITOR
  - MONITORS ADDRESS STROBE LINES
    - CREATE BUS ERROR (BERR) IF STROBE ON FOR 16 CLOCK CYCLES
    - REDUCES REQUIRED TIME TO DETECT LACK OF DATA ACKNOWLEDGE (DTACK)
- BIT 23 SET
  - SETS BIT 23 OF ADDRESS HIGH
    - FORCES DCU INTO PROM ON POWER RECOVERY
- SYNCH
  - SYNCHRONIZES DTACK / HALT / RESET SIGNALS WITH 8 MHz CLOCK

BLOCK II DIGITAL COMPUTER UNIT
SELF-CHECKING PAIR PROCESSOR

- **BUS COMPARATORS**
  - **PERFORMS A BIT-TO-BIT COMPARISON OF ADDRESS OR DATA**
- **PROM**
  - **PROVIDES CONTROLLER INITIALIZATION AND MEMORY LOAD SOFTWARE**
- **BUFFERS**
  - **PROVIDE DATA BUS NOISE REDUCTION**
  - **PROVIDE INCREASED DRIVE CAPABILITY FOR CONTROL LINES**

MAIN MEMORY


MEMSAVE
ADR/DAT STROBES
ASTRB
UDSTRB
LDSTRB
READ / WRITE
ADDRESS (12-15)
SRAM CHIP SELECT
ENABLE
INTERFACE
TRANSCEIVER
8
8
DIO
DIO
SRAM (HIGH MEMORY)
16K x 8
16K x 8
ADR
0
7
ADR
8
15
WE
OE
WE
8
11
ADDRESS (16-23)
FCX1
RDTACK
SAL (16-23)
MEMORY DECODE AND CONTROL
INTERFACE
WLB
WHB
HMR
LMR
DCU DATA BUS (16)
WE
OE
WE
SRAM (LOW MEMORY)
16K x 8
16K x 8
ADR
0
7
ADR
8
15
DIO
DIO
8
11
ADDRESS (1-11)
INTERFACE
8
8
TRANSCEIVER

BLOCK II INPUT ELECTRONICS
MAIN PROGRAM MEMORY

- SRAM
  - COMPRISED OF TWO GROUPS OF 16 K x 16 BITS
    - FIRST 8 BITS (LOW BYTE) / LAST 8 BITS (HIGH BYTE)
  - WRITE ENABLES (WE) CONTROLLED BY WRITE HIGH BYTE (WHB) AND WRITE LOW BYTE (WLB)
  - OUTPUT ENABLES (OE) CONTROLLED BY HIGH MEMORY READ (HMR) AND LOW MEMORY READ (LMR)
- INTERFACES
  - PROVIDE POWER ISOLATION FOR POWER TRANSIENT CONDITIONS
- SRAM CHIP SELECT
  - ENABLES THE SRAM CHIPS BASED UPON THE ADDRESS BITS (12-15)
- MEMORY DECODE AND CONTROL
  - ENABLES THE CHIP SELECT IF THE UPPER 8 BITS OF THE ADDRESS MATCH THE FIXED ADDRESS SPACE OF SRAM
    - UPPER 32 K - ALL ONES
    - LOWER 32 K - ALL ZEROES

BLOCK II CONTROLLER
TECHNICAL OVERVIEW

SECTION 1 - INPUT ELECTRONICS

SECTION 2 - DIGITAL COMPUTER UNIT

SECTION 3 - COMPUTER INTERFACE ELECTRONICS

SECTION 4 - OUTPUT ELECTRONICS

SECTION 5 - POWER SUPPLY

BLOCK II COMPUTER INTERFACE ELECTRONICS (CIE)
FUNCTIONS

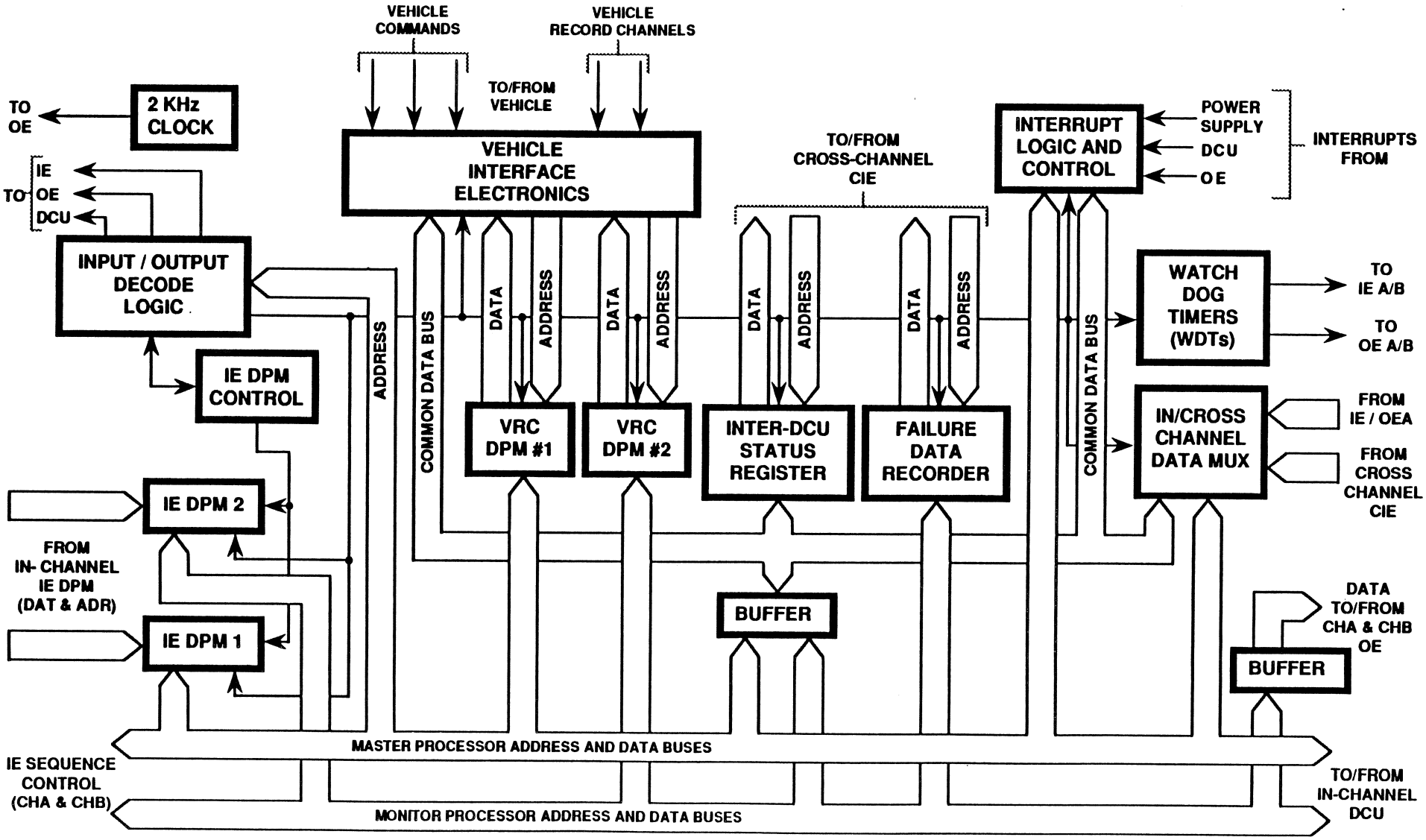
- PROVIDE THE INTERFACE CIRCUITRY FOR ENGINE-CONTROLLER COMMUNICATION
    - VIE COMMAND CHANNEL DECODER
    - VIE RECORDERS - VRCs
    - I/O CONTROL
- PROVIDE FOR THE INTERFACE BETWEEN THE DCU AND THE IE, OE AND CROSS-CHANNEL DCU
    - IE DPMs
    - IN-CHANNEL / CROSS CHANNEL DATA MUXING
    - INTER-DCU STATUS REGISTER
    - INTERRUPT CONTROL
- PROVIDE WATCH DOG TIMERS
- PROVIDE FAILURE DATA RECORDER

BLOCK II COMPUTER INTERFACE ELECTRONICS
FUNCTIONS BY CARD

- THE BLOCK II CIE CONSISTS OF SIX CARDS

FUNCTIONS	MODULE
DUAL PORT MEMORY 1	CIE1
I/O DECODE LOGIC	CIE1
INTERRUPT LOGIC	CIE2
VIE COMMAND MUXER	CIE2
REAL TIME COUNTER	CIE2
DUAL PORT MEMORY 2	CIE3
WATCH DOG TIMER 1	CIE3
VEHICLE COMMAND CHANNEL DECODER	CIE4
WATCH DOG 2	CIE4
CROSS CHANNEL DATA MUX (HIGH)	CIE4
VEHICLE RECORDER	CIE5
CROSS CHANNEL DATA MUX (LOW)	CIE5
FAILURE DATA RECORDER	CIE6

COMPUTER INTERFACE ELECTRONICS



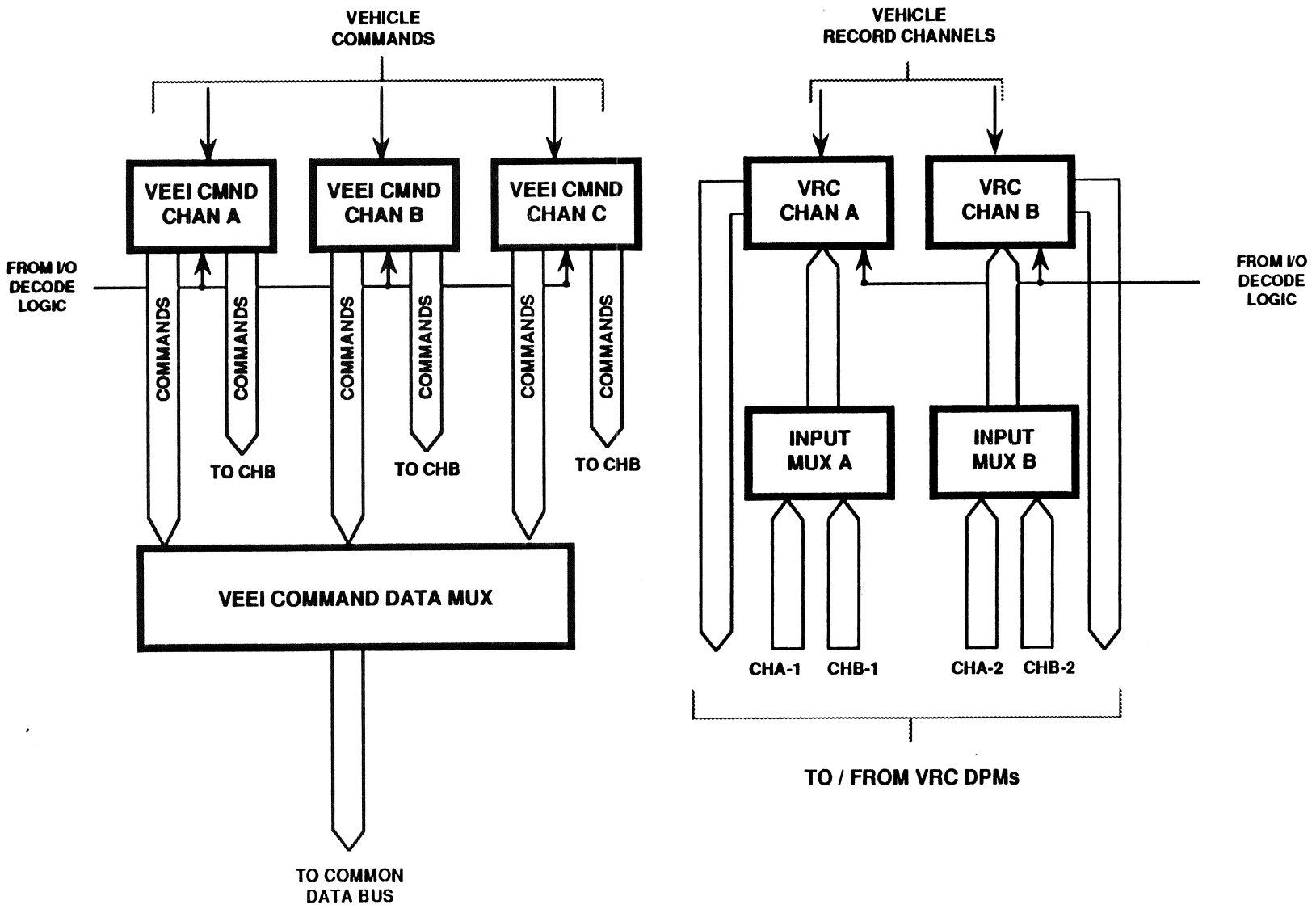
BLOCK II COMPUTER INTERFACE ELECTRONICS
FUNCTIONAL BLOCKS

- THE BLOCK II CONTROLLER COMPUTER INTERFACE ELECTRONICS IS DIVIDED INTO THI FOLLOWING FUNCTIONAL BLOCKS
  - VEHICLE INTERFACE ELECTRONICS
    - COMMAND CHANNEL DECODER
    - VEHICLE RECORDER CHANNEL
  - INTERRUPT LOGIC AND CONTROL
    - PRIORITIZES SYSTEM INTERRUPTS
    - PERFORMS MASKING OF INTERRUPTS
  - INPUT / OUTPUT DECODE LOGIC
    - PROVIDE FOR MEMORY MAPPING OF I/O ADDRESSES
    - PROVIDE FOR MUX CONTROL FOR SELF-TEST

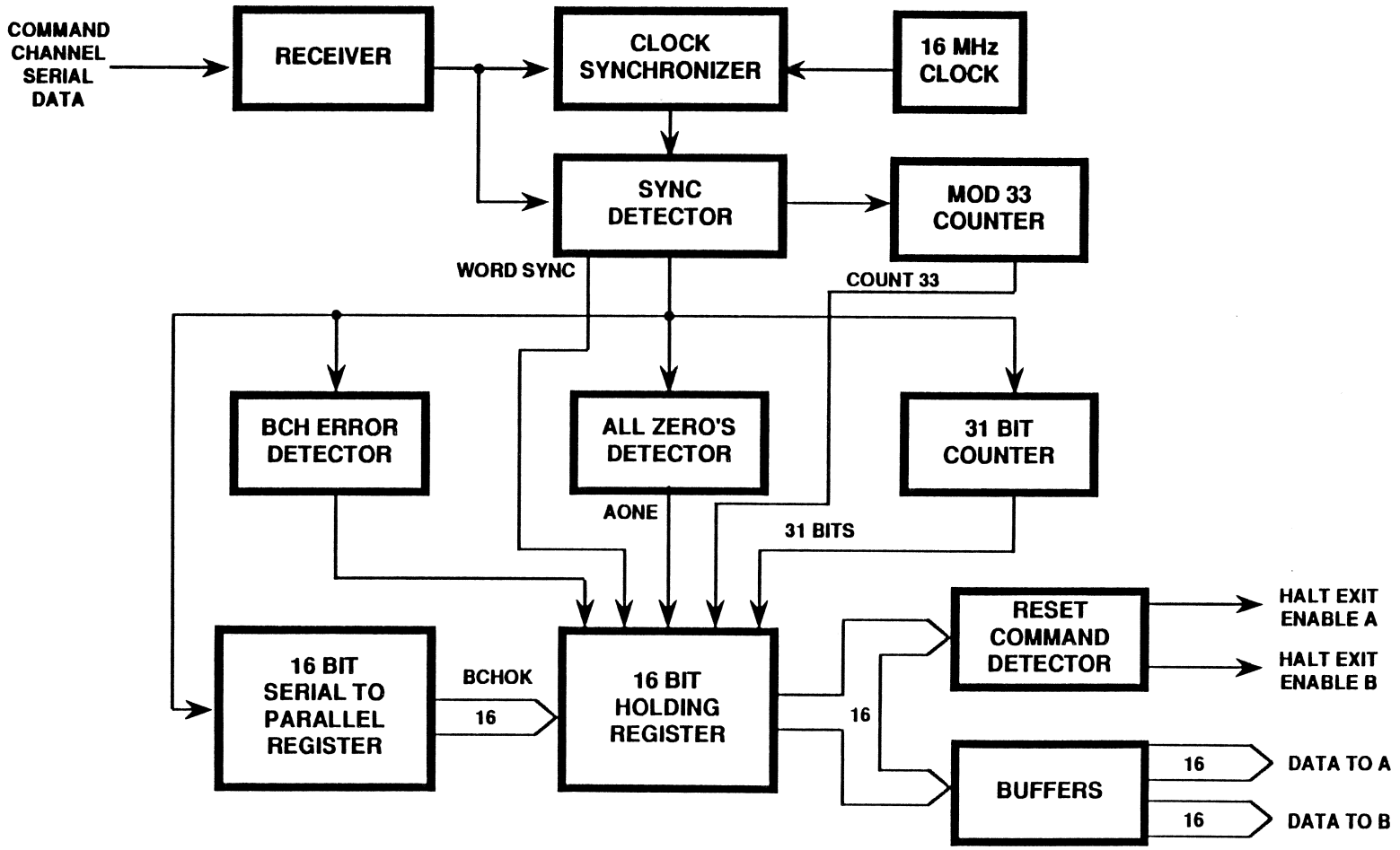
BLOCK II COMPUTER INTERFACE ELECTRONICS
FUNCTIONAL BLOCKS

- WATCH-DOG-TIMERS
    - PROVIDE TIMERS TO TEST PROCESSOR HEALTH
- IN-CHANNEL / CROSS-CHANNEL DATA MUX
    - PROVIDES FOR THE ABILITY OF CROSS CHANNEL DATA TRANSFER
- FAILURE DATA RECORDER
    - CONTAINS THE FAILURE DATA RECORDER FOR FAULT ISOLATION
- INTER-DCU STATUS REGISTER
    - PROVIDES FOR CROSS-CHANNEL SYSTEM STATUS COMMUNICATION

COMPUTER INTERFACE ELECTRONICS
VEHICLE INTERFACE ELECTRONICS



COMPUTER INTERFACE ELECTRONICS
VEHICLE INTERFACE ELECTRONICS
VEHICLE COMMAND CHANNEL



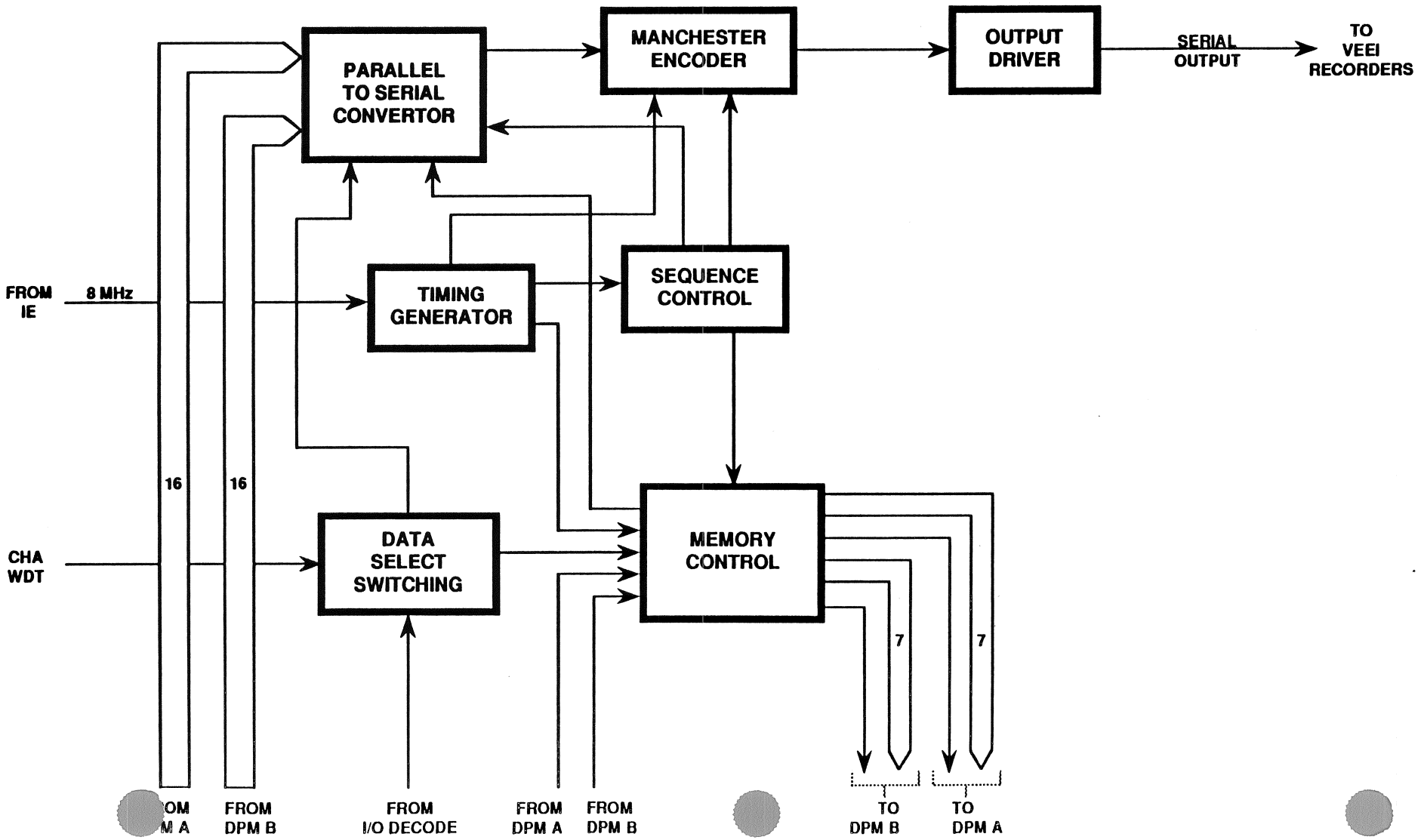
BLOCK II COMPUTER INTERFACE ELECTRONICS
VEHICLE INTERFACE ELECTRONICS
COMMAND CHANNEL DECODER

- RECEIVER / CLOCK SYNCHRONIZER
  - CONVERTS DIFFERENTIAL MANCHESTER INPUT INTO A MANCHESTER TTL DATA STREAM
- SYNC DETECTOR
  - DETECTS 2 BIT SYNC PULSE BETWEEN 31 BIT DATA WORDS
- MOD 33 COUNTER
  - COUNTS 33 BITS OF DATA, INDICATES END OF 31 BIT DATA WORD
- BCH ERROR DETECTOR
  - VERIFIES CORRECTNESS OF 31 BIT DATA WORD USING A 15 BIT BCH CODE

BLOCK II COMPUTER INTERFACE ELECTRONICS
VEHICLE INTERFACE ELECTRONICS
COMMAND CHANNEL DECODER

- ALL ZERO'S DETECTOR
  - DETECTS IF A LOGIC '1' BIT IS IN THE DATA WORD
  - CLOCKS THE HOLDING REGISTER IF A '1' IS DETECTED
- 31 BIT COUNTER
  - COUNTS THE 31 BITS OF DATA
- REGISTERS
  - CONVERT THE SERIAL DATA TO PARALLEL DATA WORD
  - TRANSFER THE DATA TO THE DCU IF IT IS A VALID DATA WORD

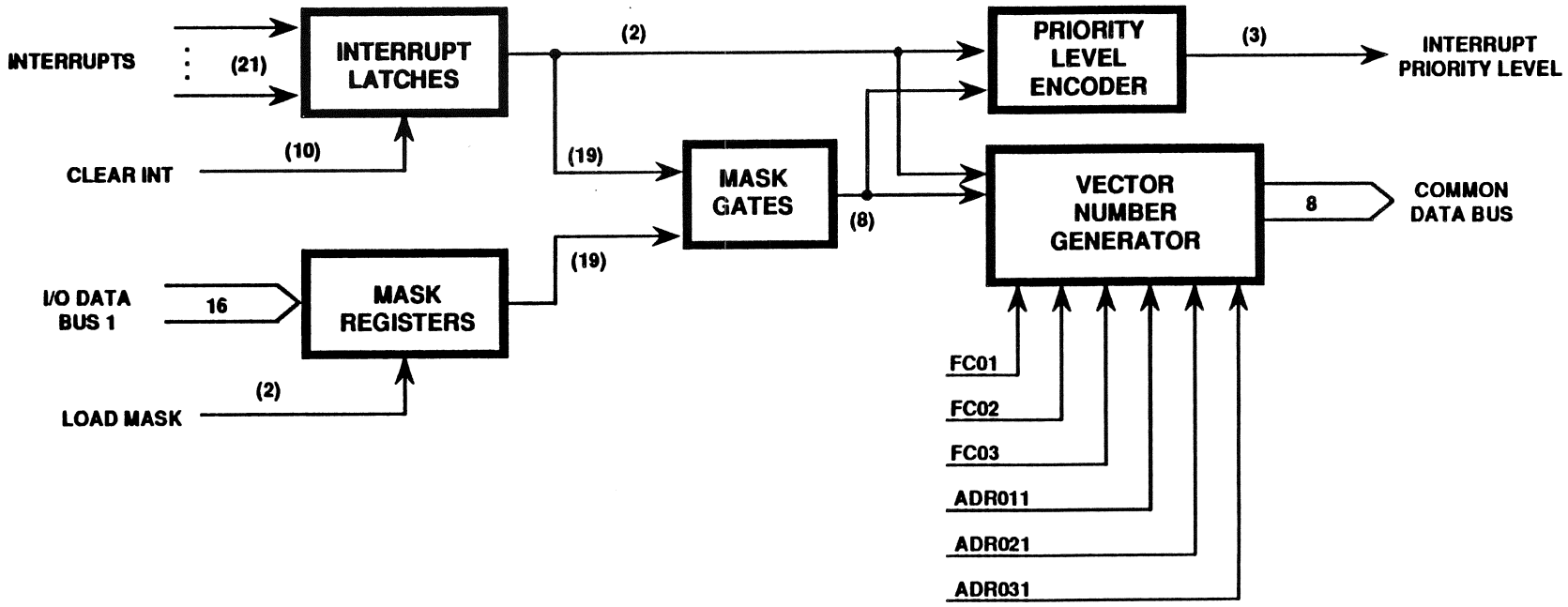
COMPUTER INTERFACE ELECTRONICS
VEHICLE INTERFACE ELECTRONICS
VEHICLE RECORDER CHANNEL



BLOCK II COMPUTER INTERFACE ELECTRONICS
VEHICLE INTERFACE ELECTRONICS
VEHICLE RECORDER CHANNEL

- MANCHESTER ENCODER
  - CONVERTS OUTPUT DIGITAL DATA TO BI-PHASE OUTPUT
- TIMING GENERATOR
  - GENERATES TIMING STREAM FOR OUTPUT DATA
- SEQUENCE CONTROL
  - CLOCKS THE OUTPUT DATA STREAM
  - READ / WRITE CONTROL
- DATA SELECT
  - SELECTS THE SOURCE OF INPUT DATA
- MEMORY CONTROLS
  - CONTROLS ADDRESSING OF DPMs

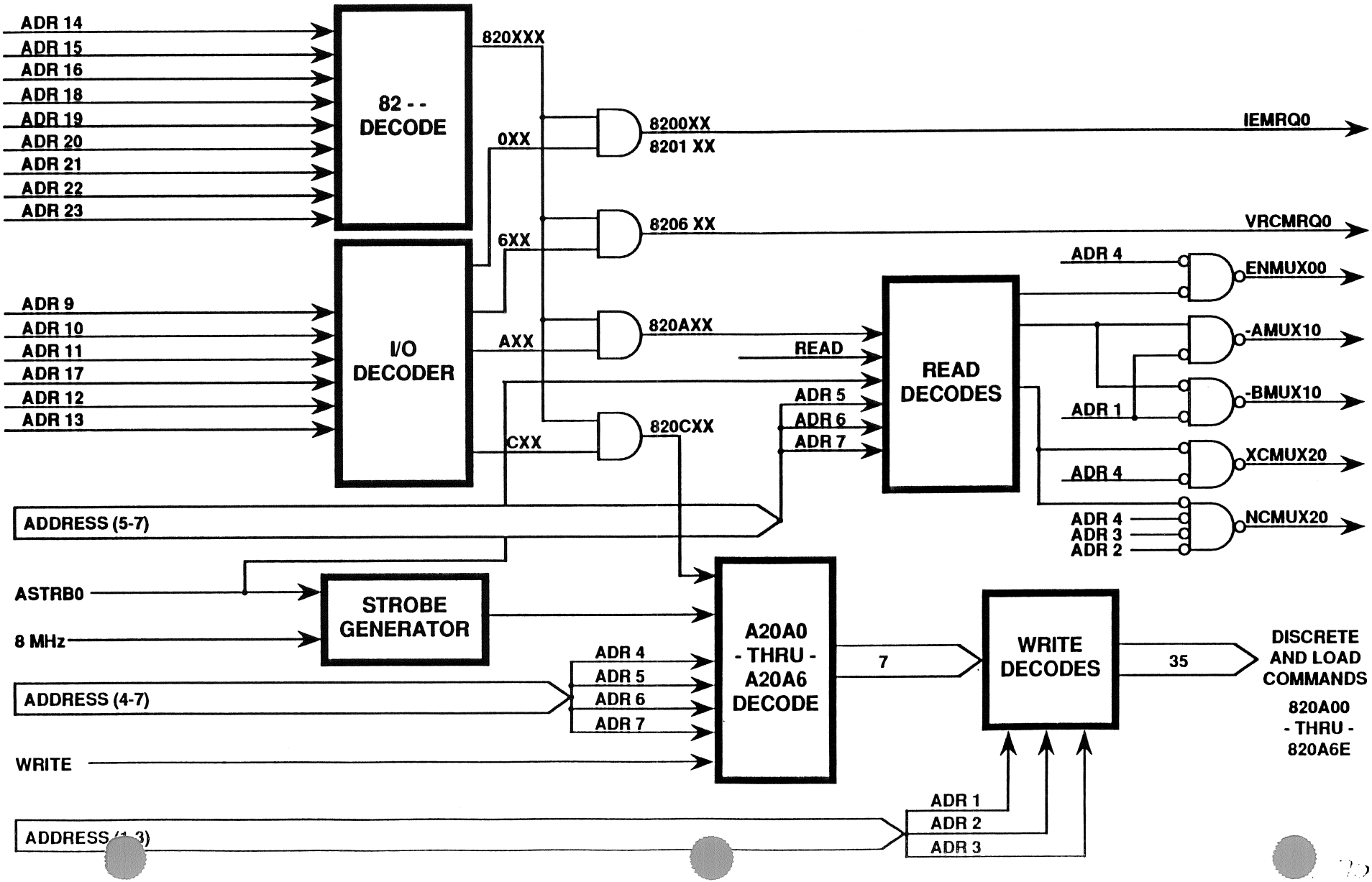
COMPUTER INTERFACE ELECTRONICS
INTERRUPT CONTROL LOGIC



BLOCK II COMPUTER INTERFACE ELECTRONICS
INTERRUPT CONTROL LOGIC

- INTERRUPT LATCHES
  - LATCHES IN INTERRUPTS FOR ENCODING
    - 12 SERVO ERROR LATCHES
    - 9 UNIQUE ERROR LATCHES
- PRIORITY LEVEL ENCODER
  - 21 INTERRUPTS ARE ENCODED INTO SEVEN LEVELS OF PRIORITY
- MASK GATES/REGISTERS
  - ALLOWS SOFTWARE TO MASK THE ENCODING OF 19 INTERRUPTS
  - THE PRI AND PFI INTERRUPTS CANNOT BE MASKED

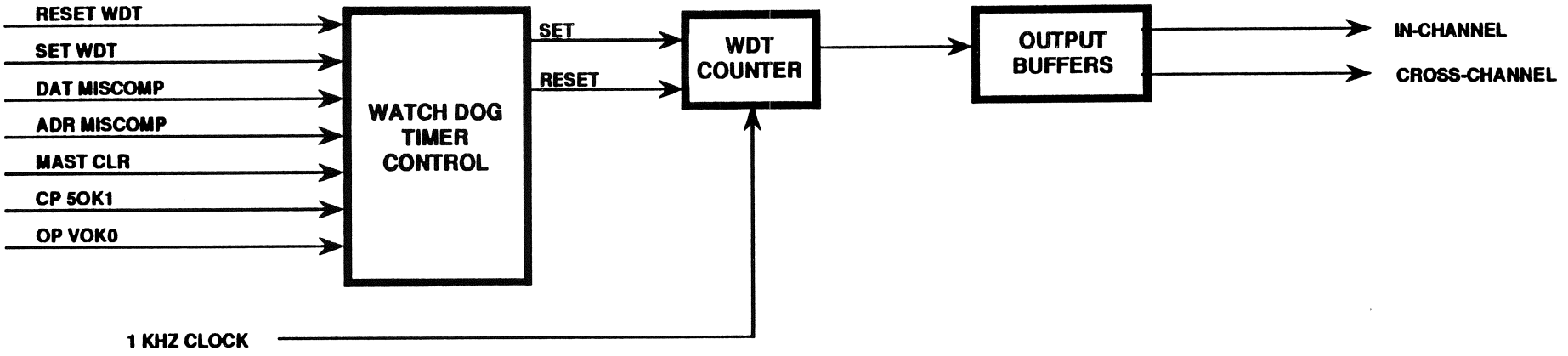
COMPUTER INTERFACE ELECTRONICS
I/O DECODE LOGIC



BLOCK II COMPUTER INTERFACE ELECTRONICS
INPUT/OUTPUT DECODE LOGIC

- 82 DECODE / IO DECODER
  - ONLY EVEN ADDRESSES ARE VALID FOR I/O DEVICE ADDRESSING
  - DETECTS I/O DEVICE ADDRESS SPACE ACCESSES
    - 820000 - 8201FF IE DUAL PORT MEMORY
    - 820600 - 8206FF VRC CHANNEL 1 & 2
    - 820A00 - 820AFF OUTPUT COMMANDS
    - 820C00 - 820CFF INPUT COMMANDS
- READ DECODE LOGIC
  - ENABLES THE FOLLOWING MUXES
    - VEEI COMMAND/DATA MUX (ENMUXOO)
    - CH-A DATA MUX (ENMUX00)
    - SELF-TEST MUX (AMUX10)
    - CROSS-CHANNEL SELF-TEST MUX (BMUX10)
    - CROSS CHANNEL COMMUNICATION (NCMUX20,XCMUX20)
- WRITE DECODES
  - CONTROLS THE WRITING TO DISCRETE DEVICES (ON/OFF REGISTERS, IE SEQUENCE CONTROL, SET/RESET WDTs, INTERRUPT CLEARS, ETC.)

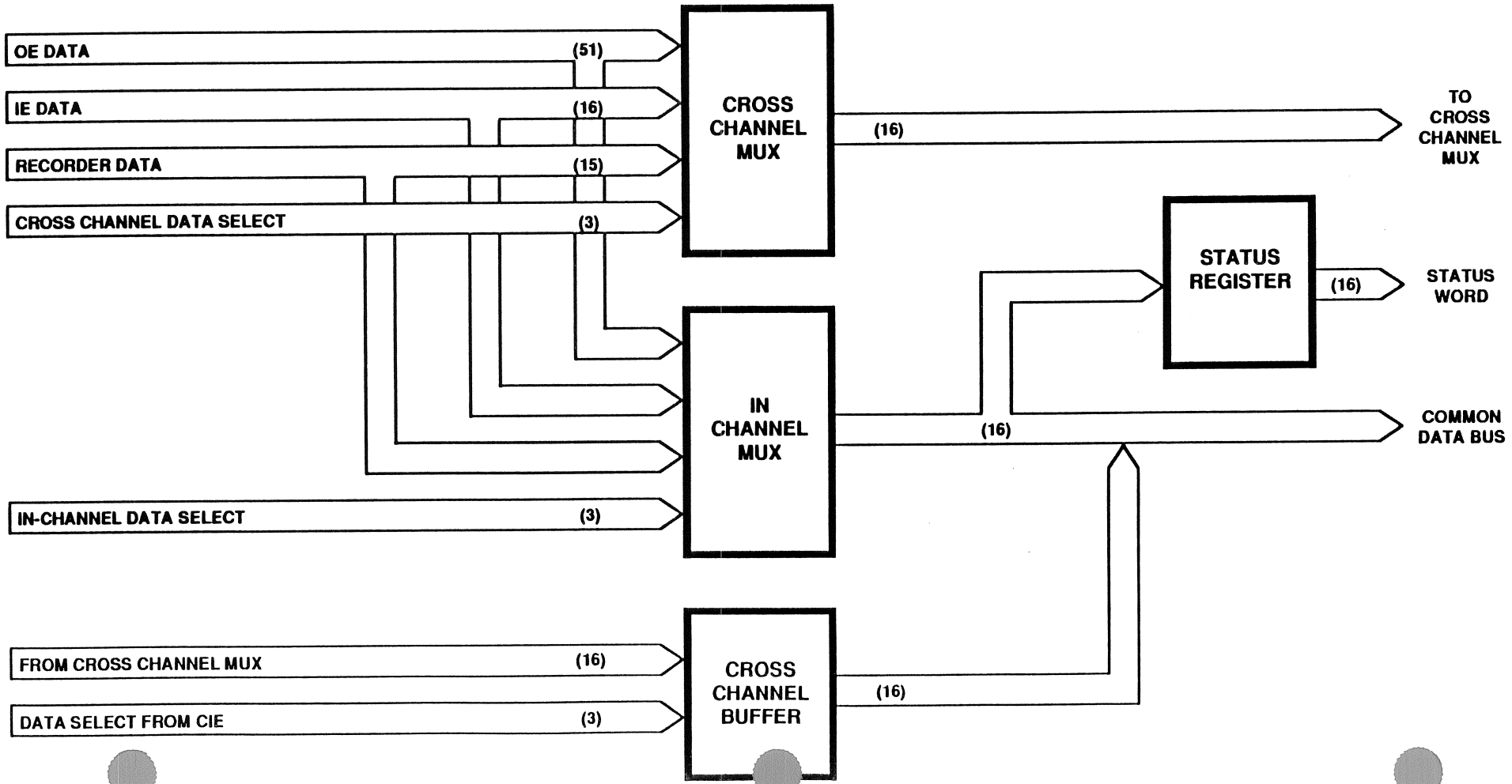
COMPUTER INTERFACE ELECTRONICS
WATCH DOG TIMER



BLOCK II ICOMPUTER INTERFACE ELECTRONICS
WATCH DOG TIMERS

- WATCH DOG CONTROL
    - RECEIVES INPUT SIGNALS FROM DCU AND POWER SUPPLY
- WDT COUNTER
    - PROVIDES TIMING FOR WATCH DOG COUNTER
- BUFFERS
    - OUTPUTS THE STATUS OF THE WDT TO BOTH CHANNELS

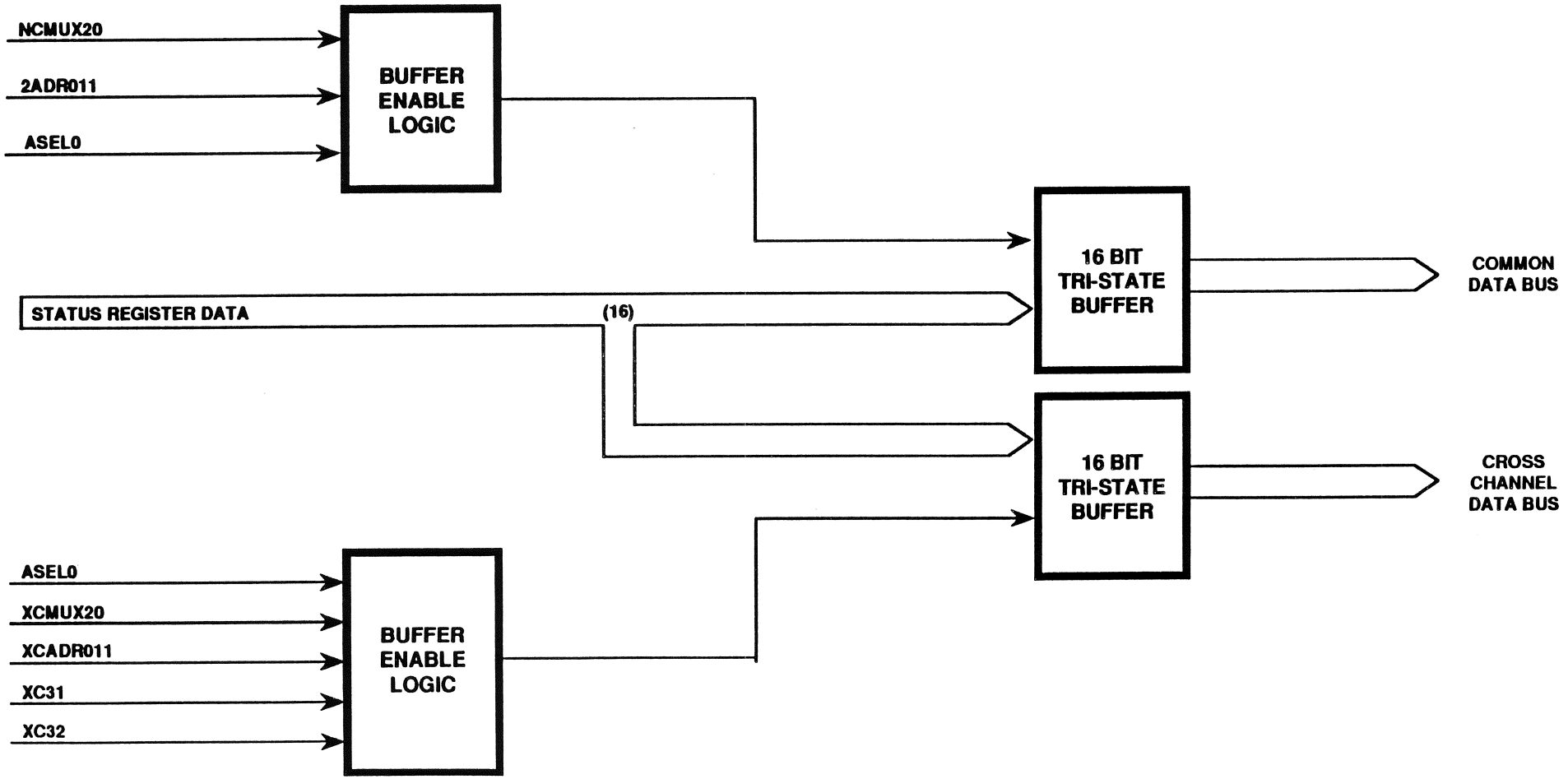
COMPUTER INTERFACE ELECTRONICS
IN / CROSS CHANNEL DATA MUX



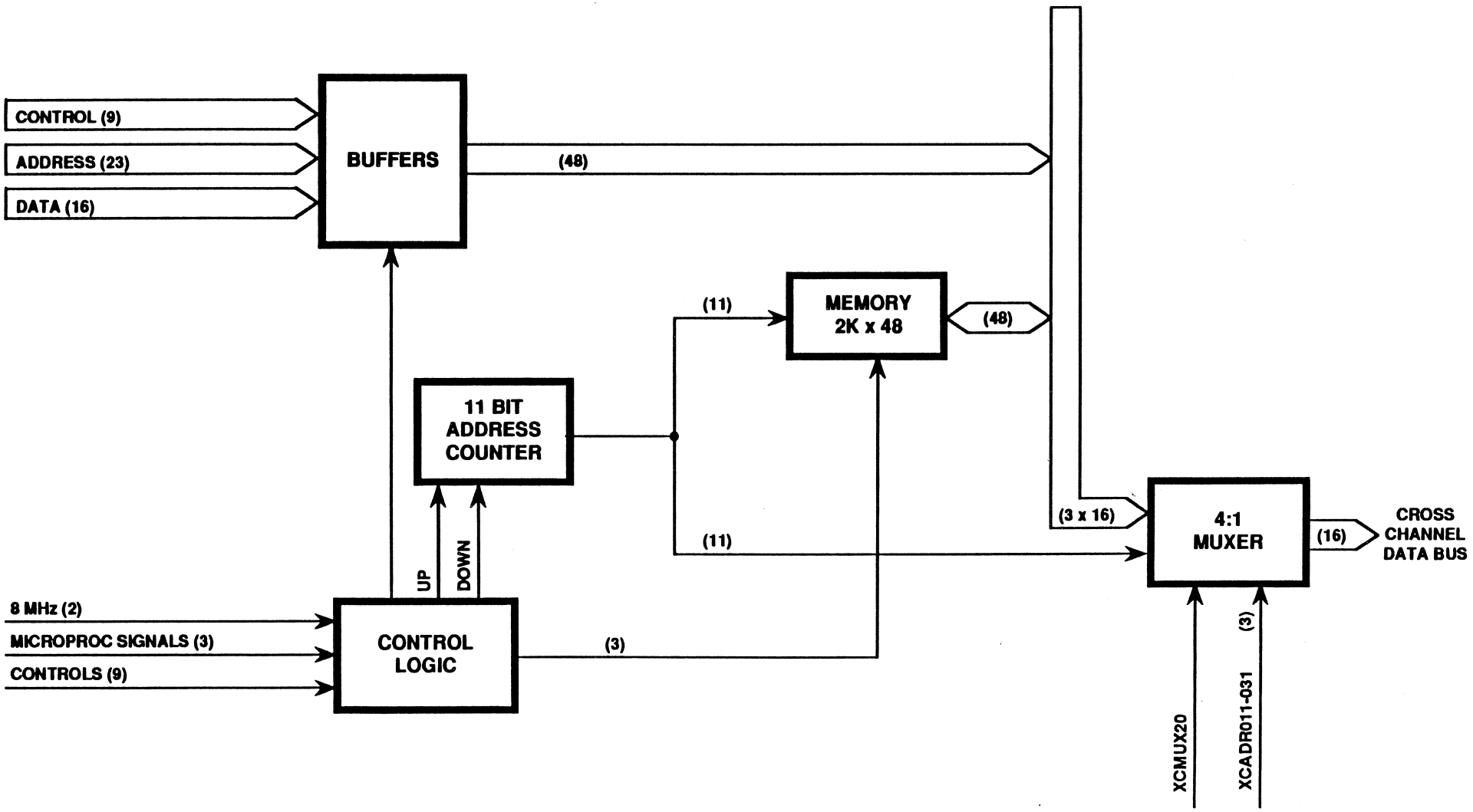
BLOCK II COMPUTER INTERFACE ELECTRONICS
IN-CHANNEL/CROSS-CHANNEL DATA MUX

- CROSS-CHANNEL MUX
    - ROUTES IN-CHANNEL SELF TEST DATA TO CROSS CHANNEL
- IN-CHANNEL MUX
    - ROUTES IN-CHANNEL SELF TEST DATA TO IN-CHANNEL
- CROSS-CHANNEL BUFFER
    - RECEIVES CROSS-CHANNEL DATA FROM CROSS-CHANNEL DATA MUX
- STATUS REGISTER
    - HOLDING REGISTER FOR INTER-DCU STATUS REGISTER

COMPUTER INTERFACE ELECTRONICS
INTER-DCU STATUS REGISTER



COMPUTER INTERFACE ELECTRONICS
FAILURE DATA RECORDER



BLOCK II COMPUTER INTERFACE ELECTRONICS
FAILURE DATA RECORDER

- MEMORY 2K * 48
    - STORES DCU DATA OF MONITOR PROCESSOR
- 11 BIT ADDRESS COUNTER
    - CYCLES THROUGH THE 2K MEMORY ON A CONTINUOUS BASIS
    - CONTROLLED BY THE CONTROL LOGIC
- INHIBITED
    - WRITING IS INHIBITED UPON
        - SCP INTERRUPT
        - SOFTWARE COMMAND
        - MASTER CLEAR
        - GSE COMMAND
    - WRITING IS ENABLED UPON
        - SOFTWARE COMMAND
        - GSE COMMAND

BLOCK II CONTROLLER
TECHNICAL OVERVIEW

SECTION 1 - INPUT ELECTRONICS

SECTION 2 - DIGITAL COMPUTER UNIT

SECTION 3 - COMPUTER INTERFACE ELECTRONICS

SECTION 4 - OUTPUT ELECTRONICS

SECTION 5 - POWER SUPPLY

BLOCK II OUTPUT ELECTRONICS (OE)
FUNCTIONS

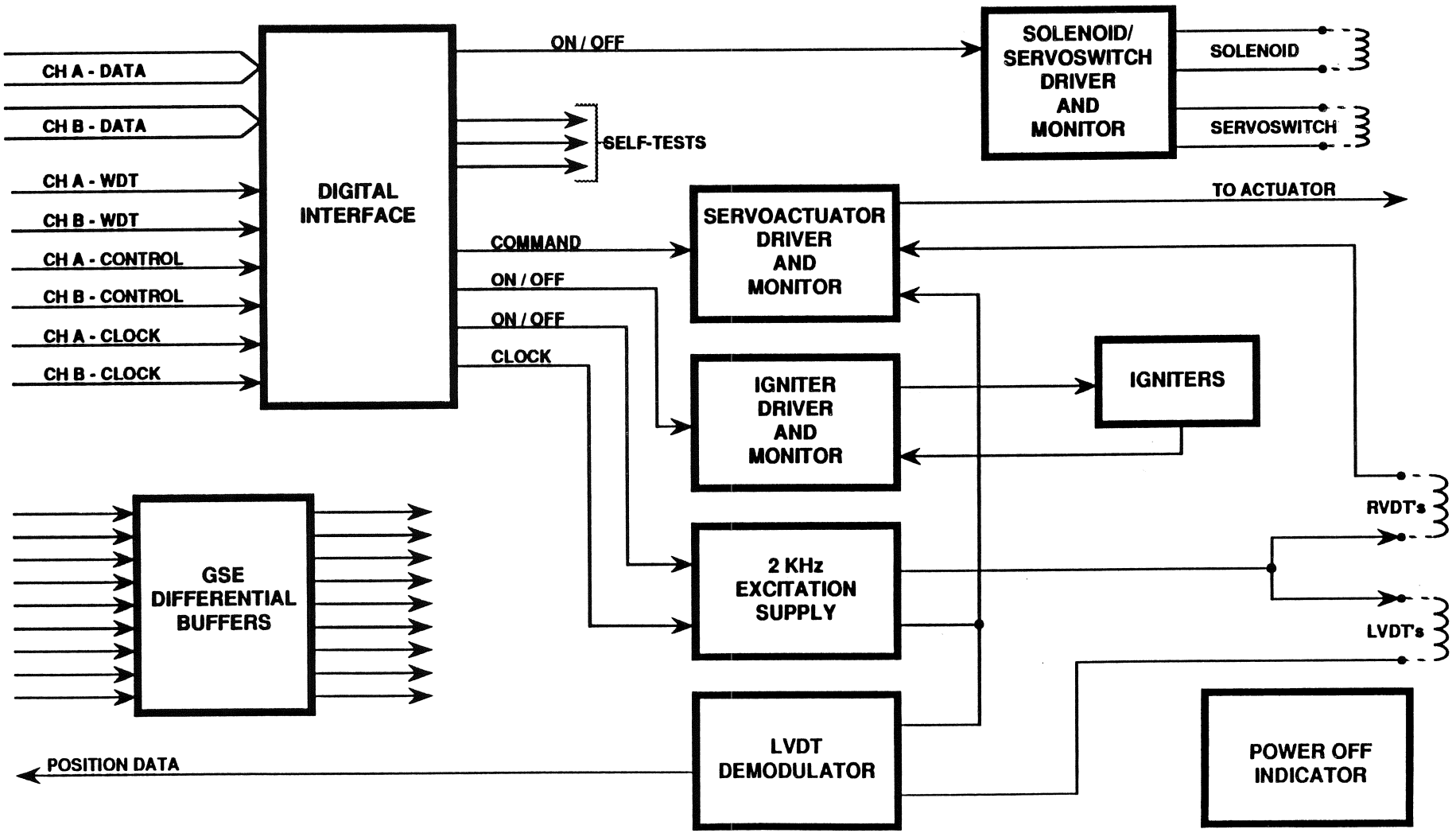
- PROVIDE COMMAND INTERFACE BETWEEN DCU AND ENGINE CONTROL DEVICES
- PROVIDE ENGINE CONTROL DEVICE POSITION INFORMATION TO DCU
- MONITORS RESPONSE OF ENGINE CONTROL DEVICE DRIVERS TO COMMANDS
- MONITORS ENGINE IGNITION
- MONITORS +5 VDC & +15 VDC TO INITIATE CHANNEL SHUTDOWN UPON FAILURE
- PROVIDES 2 KHz EXCITATION TO RVDT & LVDT VALVE POSITION DEVICES
- PROVIDE POWER OFF INDICATION OF THE 28 VDC ORBITER POWER BUS
- PROVIDE GROUND SUPPORT EQUIPMENT (GSE) DIFFERENTIAL BUFFERS

BLOCK II OUTPUT ELECTRONICS
FUNCTIONS BY CARD

- THE BLOCK II OE CONSISTS OF SEVEN CARDS

FUNCTIONS	MODULE
DIGITAL INTERFACE	OE1
POWER OFF INDICATOR	OE1
GSE DRIVERS	OE1
UNDERVOLTAGE MONITOR	OE1
SERVOSWITCH DRIVERS/MONITORS (FAIL-SAFE)	OE2
SOLENOID DRIVERS/MONITORS (POGO PRECHARGE, EMSD, PBP S/D)	OE2
LVDT DEMODULATOR AND FILTERS	OE3
SERVOACTUATOR DRIVERS/MONITOR (MFV & OPOV)	OE4
SERVOACTUATOR DRIVERS/MONITOR (MOV, FPOV & CCV)	OE5
IGNITER DRIVER/MONITOR	OE6
RVDT/LVDT EXCITATION SOURCE	OE6
SERVOSWITCH DRIVER/MONITORS (FAIL-OP)	OE7
SOLENOID DRIVER/MONITORS (BLEED VALVES, FUEL SYS PRG, HPOT IMSL)	OE7

OUTPUT ELECTRONICS



BLOCK II OUTPUT ELECTRONICS
FUNCTIONAL BLOCKS

- THE BLOCK II CONTROLLER OUTPUT ELECTRONICS IS DIVIDED INTO THE FOLLOWING FUNCTIONAL BLOCKS
  - DIGITAL INTERFACE
    - CONTAINS DATA SELECT LOGIC (CHANNEL IN CONTROL)
    - SIX LATCHING 12 BIT DIGITAL TO ANALOG (D/A) CONVERTORS
    - THREE 12 BIT ON / OFF COMMAND REGISTERS
    - SELECTS RVDT/LVDT 2 KHz EXCITATION SOURCE CLOCK (CH A OR B)
    - PROVIDES POWER SAFETY CONTROL
  - SERVOACTUATOR DRIVERS AND MONITORS
    - PROVIDE RVDT POSITION INFORMATION TO IE FOR A/D CONVERSION
    - PROVIDE CLOSED LOOP ACTUATOR POSITIONING IN RESPONSE TO COMMAND INPUT
    - PROVIDE MONITORING OF ACTUATOR RESPONSE TO COMMAND INPUT

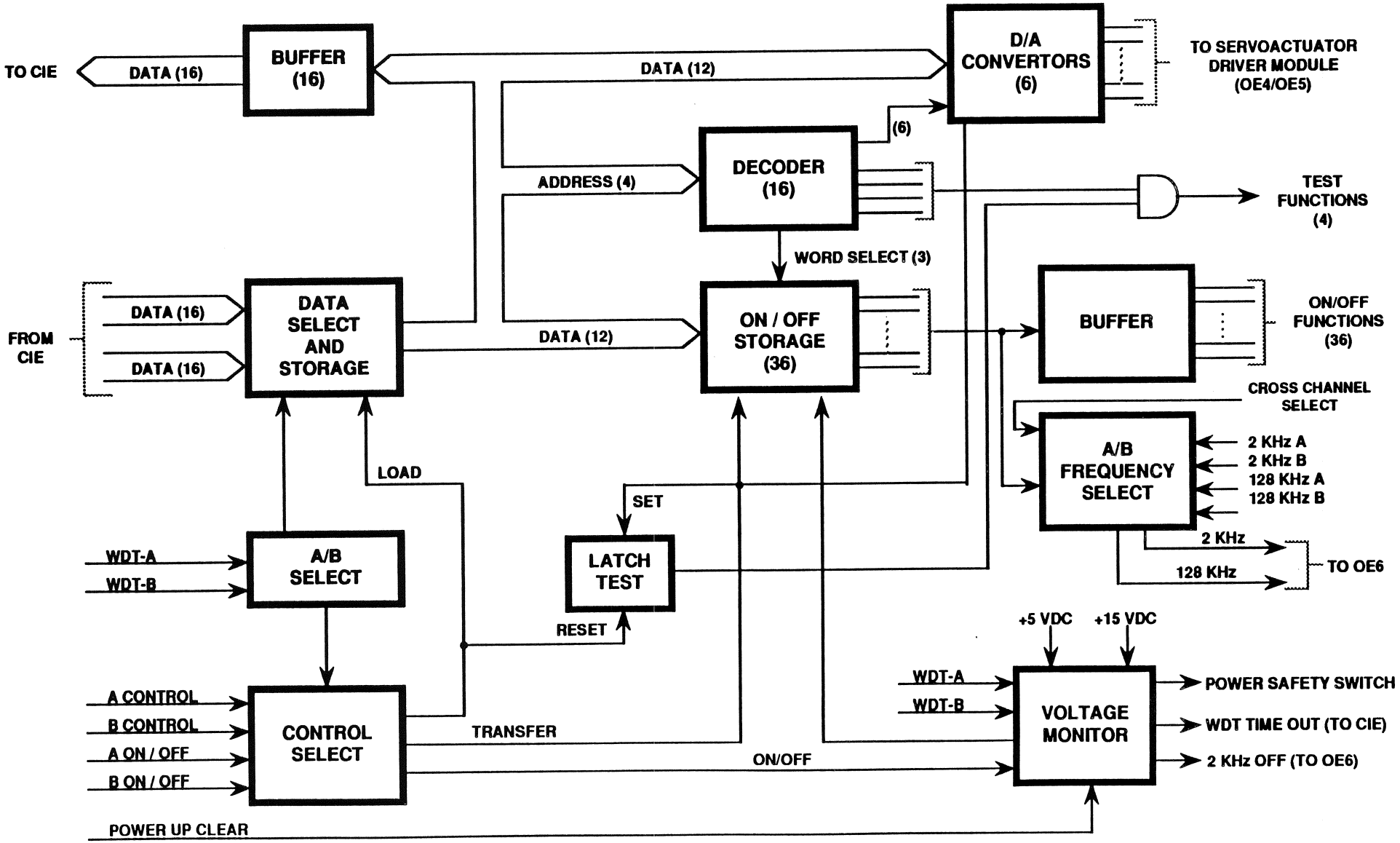
BLOCK II OUTPUT ELECTRONICS
FUNCTIONAL BLOCKS

- SOLENOID / SERVOSWITCH DRIVERS AND MONITORS
  - SOLENOID DRIVER
    - LIMITS CURRENT DURING PULL IN AND SHORT CIRCUIT MODE
    - ACTS AS VOLTAGE SWITCH DURING HOLD MODE
  - SOLENOID MONITOR
    - INDICATES TRUE WHEN CURRENT EXCEEDS REFERENCE LEVEL
  - SERVOSWITCH DRIVER
    - SUPPLIES ENERGIZE CURRENT TO SERVOSWITCHES
  - SERVOSWITCH MONITOR
    - INDICATES WHEN CURRENT RISES TO MINIMUM ENERGIZING LEVEL
    - INDICATES WHEN CURRENT FALLS TO MAXIMUM DE-ENERGIZING LEVEL

BLOCK II OUTPUT ELECTRONICS
FUNCTIONAL BLOCKS

- IGNITER DRIVERS AND MONITORS
    - IGNITER DRIVERS
        - PROVIDES SIGNAL TO TURN ON THREE IGNITERS
        - LIMIT OUTPUT CURRENT TO THE IGNITERS (0.049 AMPS)
    - IGNITER MONITORS
        - INDICATES TRUE WHEN IGNITERS PULSES ARE WITHIN NORMAL SPECIFICATION
- RVDT / LVDT EXCITATION SUPPLY
    - PROVIDES SYNTHESIZED 2 KHz SINE WAVE
- LVDT DEMODULATOR
- POWER OFF INDICATOR
    - MONITORS THE 28 VDC BUS

OUTPUT ELECTRONICS
DIGITAL INTERFACE ELECTRONICS



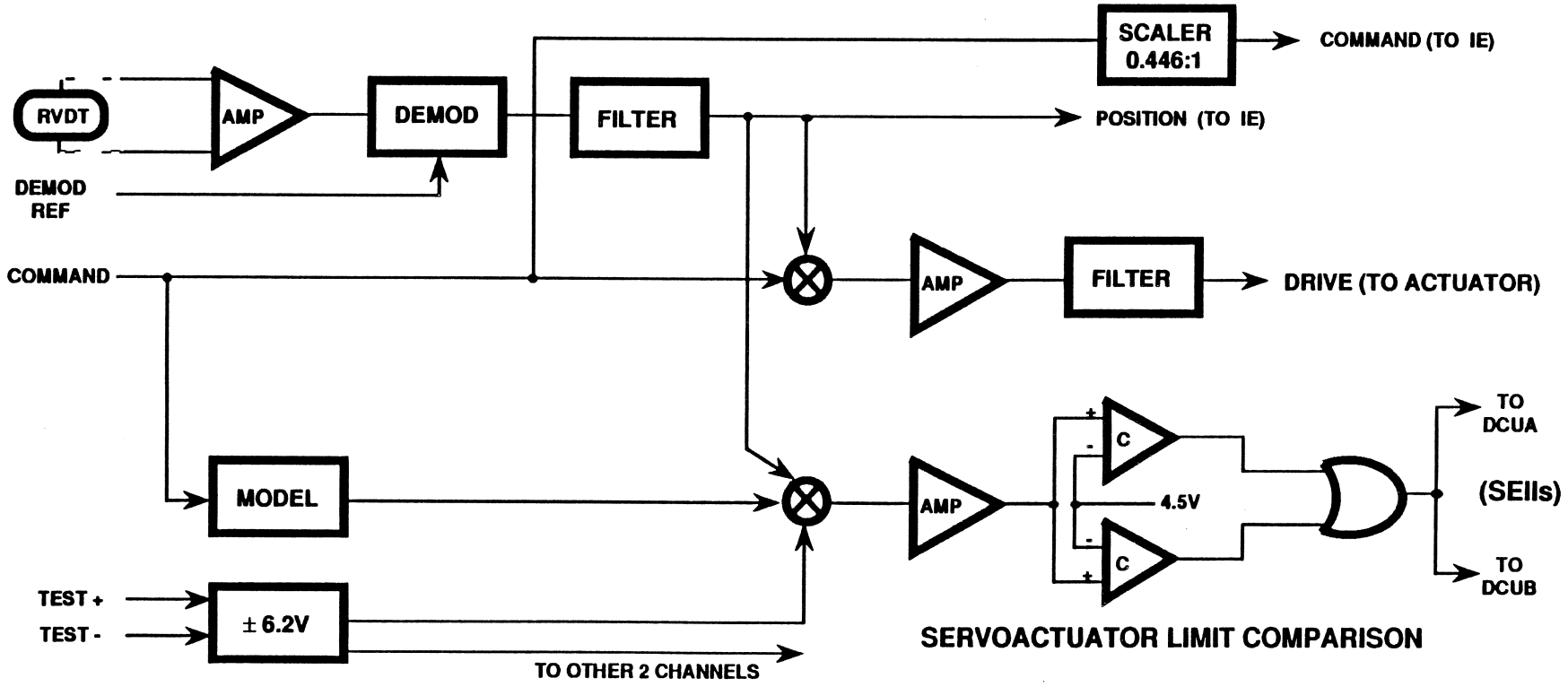
BLOCK II OUTPUT ELECTRONICS
DIGITAL INTERFACE

- A/B SELECT LOGIC
  - SELECTS CHANNEL IN CONTROL BASED UPON THE WATCH DOG TIMERS
  - THE DATA SELECT AND STORAGE
    - SELECTS DATA FOR USE BASED UPON A/B SELECT
    - PLACES DATA INTO THE OE REGISTER
  - CONTROL SELECT
    - SELECTS CONTROL SIGNALS BASED UPON A/B SELECT
- DECODER
  - UTILIZES THE FOUR LEAST SIGNIFICANT BITS OF THE OE REGISTER FOR COMMAND DECODING
- ON / OFF STORAGE
  - THREE 12-BIT REGISTERS THAT ARE ENABLED BY THE WORD SELECT FROM THE DECODER

BLOCK II OUTPUT ELECTRONICS
DIGITAL INTERFACE

- DIGITAL TO ANALOG CONVERTORS (D/As)
  - SIX 12-BIT D/As WHICH OUTPUT AN ANALOG VOLTAGE OF 0 - 10 VOLTS
  - ACTIVE D/A IS SELECTED BY THE DECODER
- A/B FREQUENCY SELECT
  - SELECTS THE 2KHz / 128KHz SOURCE FOR THE RVDT/LVDT EXCITATION
- VOLTAGE MONITOR
  - MONITORS THE +5 VDC, +15 VDC FOR UNDERVOLTAGE CONDITION
  - SET POWER SAFETY SWITCH TRUE IF UNDERVOLTAGE OCCURS

OUTPUT ELECTRONICS
SERVOACTUATOR DRIVER/MONITOR



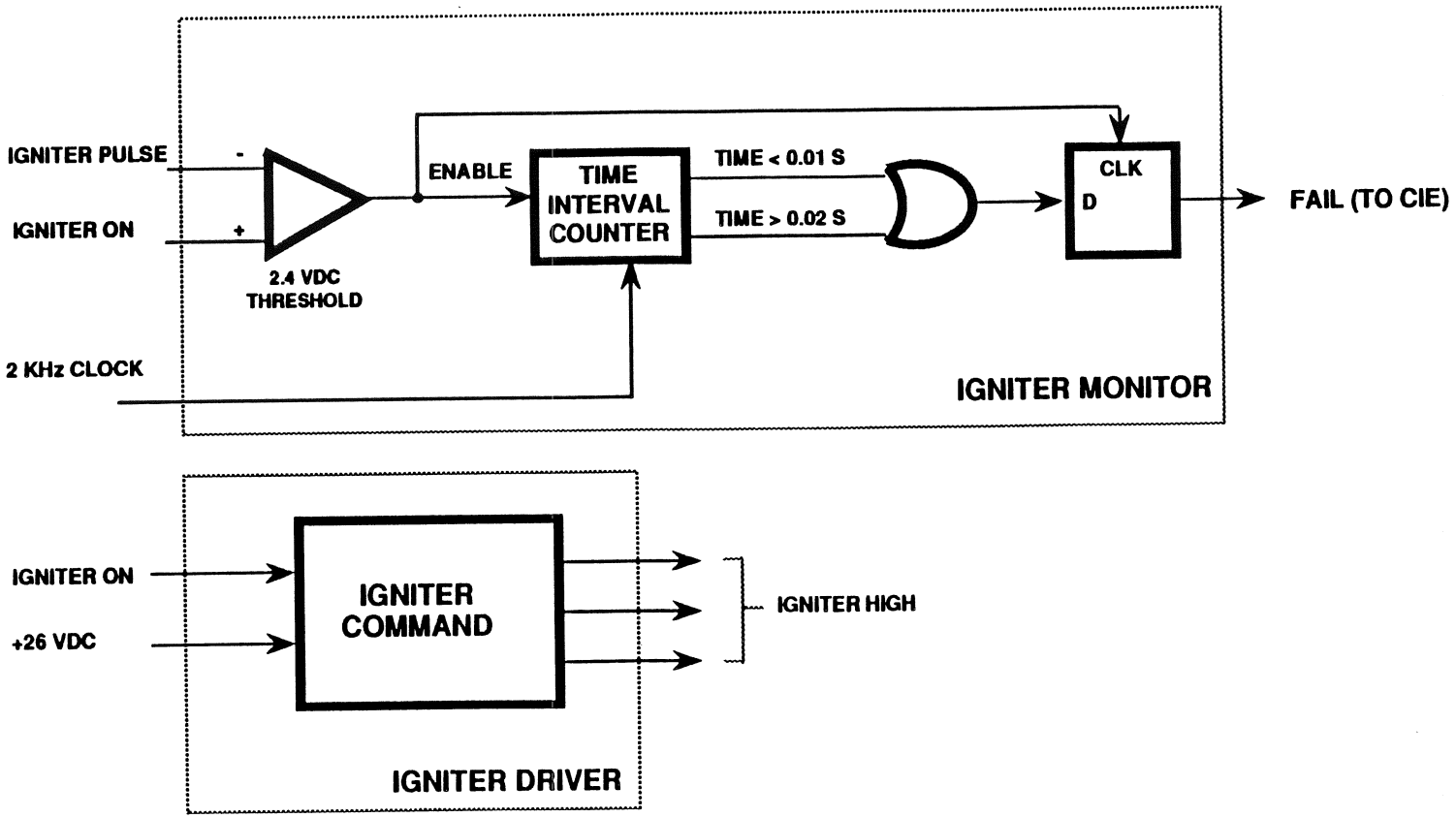
BLOCK II OUTPUT ELECTRONICS
SERVOACTUATOR DRIVER / MONITOR

- RVDT CONDITIONING LOGIC
  - THE PRE-AMP PROVIDES A GAIN OF 2.369 V/V
  - THE DEMODULATOR PROVIDES THE AMPLITUDE OF THE 2 KHz SINEWAVE
  - THE FILTER IS A SECOND ORDER LOW PASS FILTER WHICH ELIMINATES THE 2 KHz RIPPLE
- SERVOACTUATOR DRIVE
  - COMMAND AND RVDT POSITION ARE FED INTO THE SUMMING NETWORK
  - THE SUMMING NETWORK OUTPUTS AN ERROR SIGNAL TO THE DRIVE AMPLIFIER

BLOCK II OUTPUT ELECTRONICS
SERVOACTUATOR DRIVER / MONITOR

- SERVOACTUATOR LIMIT COMPARISON
  - VALVE MODEL
    - RECEIVES INPUT COMMAND
    - GENERATES A PROPORTIONAL RESPONSE OF AN IDEAL ACTUATOR
  - SUMMING NETWORK
    - SUM MODEL OUTPUT WITH REAL ACTUATOR POSITION
    - OUTPUTS ERROR SIGNAL TO LIMIT COMPARATORS
  - LIMIT COMPARATORS
    - COMPARE ERROR SIGNAL TO ESTABLISHED TRIP LEVELS (CHA: 6%, CHB: 10%)
    - PROVIDES SERVOACTUATOR INTERRUPT (SEII) WHEN OUTSIDE OF THE LIMITS (± 4.5 VDC)
    - A TEST VOLTAGE OF ±6.2 VOLTS CAN BE USED TO CREATE AN SEII

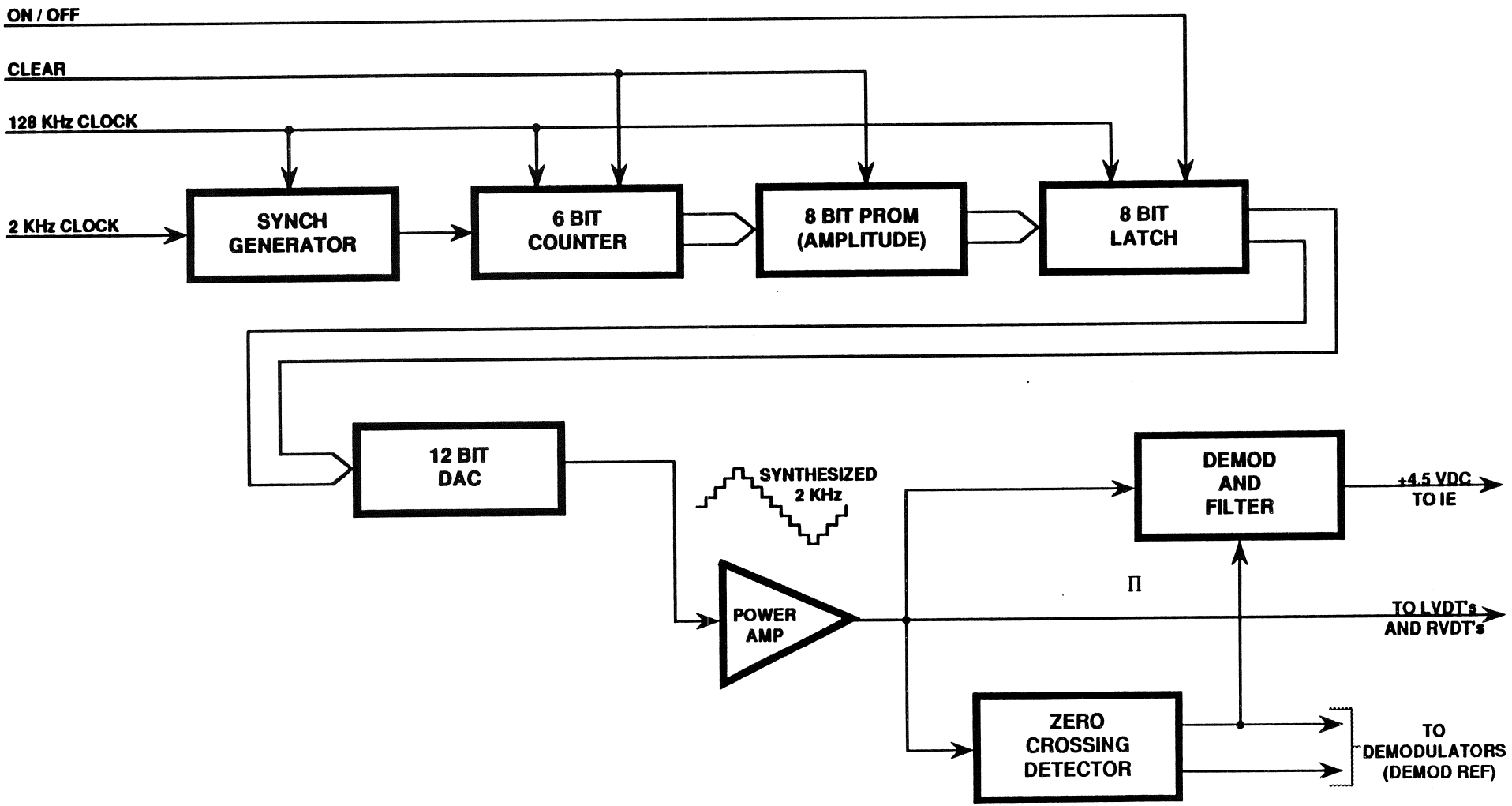
OUTPUT ELECTRONICS
IGNITER DRIVER / MONITOR



BLOCK II OUTPUT ELECTRONICS
IGNITER DRIVER / MONITOR

- IGNITER DRIVER
  - PROVIDES SIGNAL DRIVE (+26 VDC) TO ENERGIZE THREE IGNITERS
  - LIMITS OUTPUT CURRENT (0.049 A) TO THE IGNITERS
- IGNITER MONITOR
  - MONITORS IGNITER PULSE
    - AMPLITUDE (GREATER THAN 2.4 VDC)
    - FREQUENCY (50 TO 100 Hz)
  - PROVIDES FAILURE INDICATION IF LIMITS ARE EXCEEDED

OUTPUT ELECTRONICS
2 KHz GENERATION



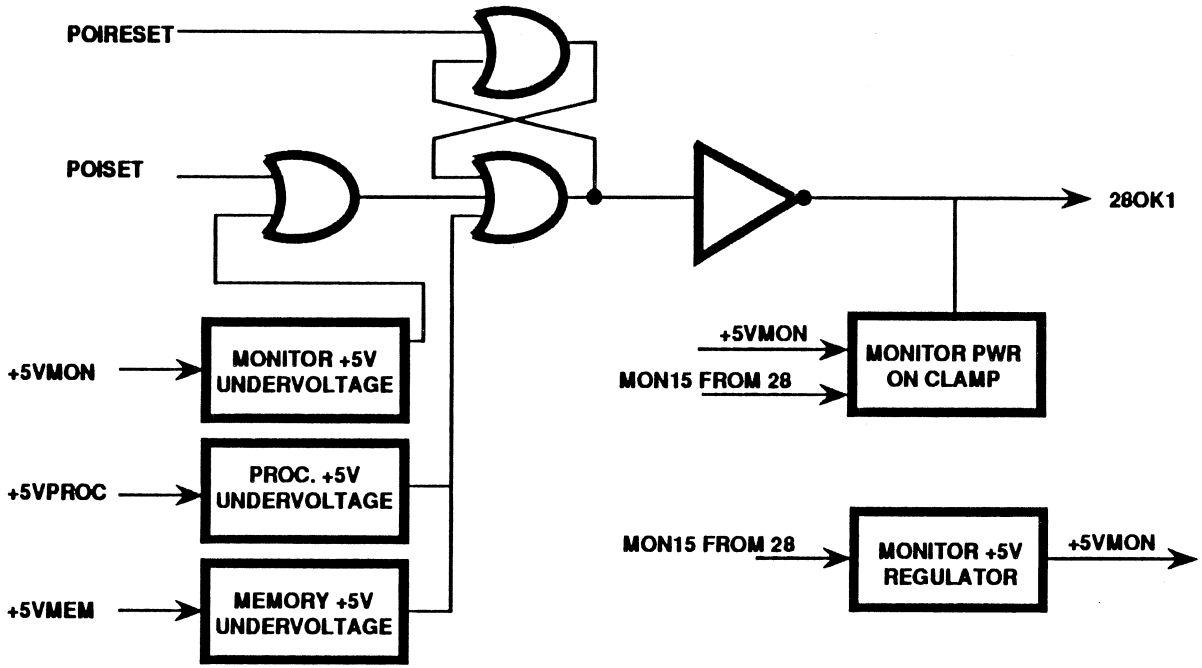
BLOCK II OUTPUT ELECTRONICS
2 KHz EXCITATION

- 2 KHz GENERATION
  - SIX BIT COUNTER
    - CLOCKED BY 128 KHz SQUARE WAVE
    - OUTPUTS THE ADDRESS TO THE 8 BIT PROM
    - RESET BY SYNCH GENERATOR
  - 8 BIT PROM
    - CONTAINS 64 DATA POINTS WHICH REPRESENT A 2 KHz SINEWAVE
    - PROVIDES AMPLITUDE TO THE A/D CONVERTOR
  - 12 BIT D/A CONVERTOR
    - CONVERTS THE DIGITAL AMPLITUDE DATA FROM THE PROM TO CREATE AN ANALOG 2 KHz SINEWAVE
    - THE OUTPUT IS AMPLIFIED AND SENT TO THE RVDT's & LVDT's

BLOCK II OUTPUT ELECTRONICS
2 KHz EXCITATION

- ZERO CROSSING DETECTOR
    - GENERATES TWO 2 KHz SQUARE WAVES (ONE IN PHASE / ONE OUT OF PHASE)
- DEMODULATOR AND FILTER
    - PROVIDES THE IE WITH THE AMPLITUDE OF THE SYNTHESIZED 2 KHz SINEWAVE

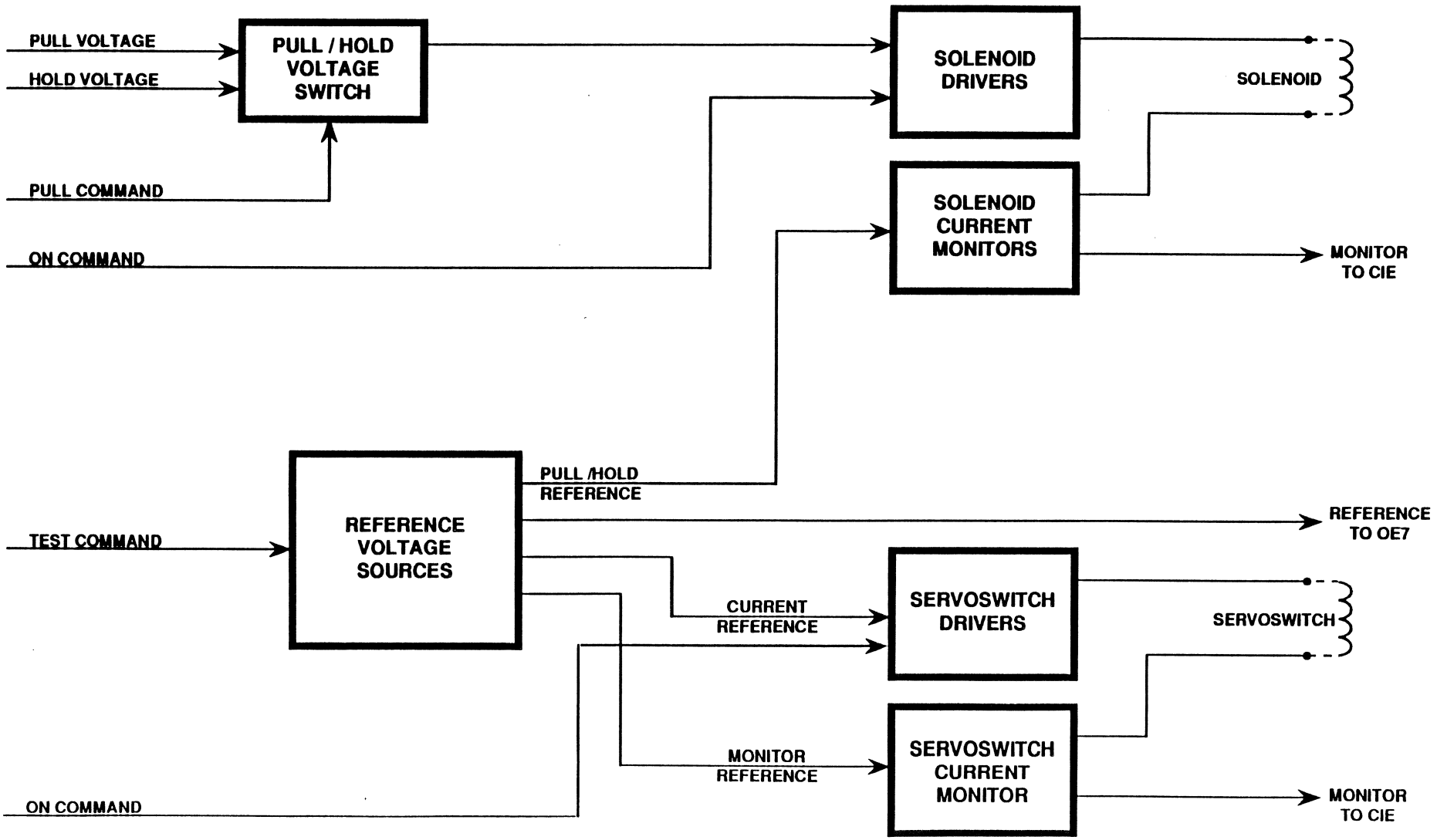
OUTPUT ELECTRONICS
POWER OFF INDICATOR



BLOCK II OUTPUT ELECTRONICS
POWER OFF INDICATOR

- UNDERVOLTAGE MONITORS
  - MONITORS (PROCESOR, MEMORY, AND MONITOR) +5 VDC
  - CREATE A POWER OFF INTERRUPT (POI) IF AN UNDERVOLTAGE CONDITION OCCURS
- MONITOR POWER CLAMP
  - CREATE A POI IF THE 28 SUPPLY HAS GONE DOWN WHILE THE 115 VAC BUS IS DOWN
  - CLAMPS 28OK1 TO LOW UNTIL ALL VOLTAGE LEVELS ARE ESTABLISHED

OUTPUT ELECTRONICS
SOLENOID & SERVOSWITCH DRIVERS AND MONITORS



BLOCK II OUTPUT ELECTRONICS
SOLENOID & SERVOSWITCH DRIVERS / MONITORS

- SOLENOID VOLTAGE SWITCH
  - PASSES PULL AND HOLD VOLTAGE LEVELS TO THE SOLNOID DRIVER
  - CONTROLLED BY PULL COMMAND FROM THE DCU
    - ASSERTED LOW REPRESENTS PULL (HIGH --> HOLD)
- SOLENOID DRIVER
  - OUTPUTS PULL/HOLD VOLTAGES (+29,+24/+16,+8) TO THE SOLENOIDS
  - PROVIDES CURRENT LIMITING OF 1 AMP
- SOLENOID CURRENT MONITOR
  - COMPARES OUTPUT CURRENT TO A REFERENCE LEVEL
  - OUTPUTS FAILURE STATUS TO CIE

BLOCK II OUTPUT ELECTRONICS
SOLENOID & SERVOSWITCH DRIVERS / MONITORS

- **SERVOSWITCH DRIVERS**
  - **PROVIDES CURRENT REGULATION (26 mA) TO THE SERVOSWITCHES**
- **SERVOSWITCH MONITORS**
  - **MONITOR STATUS OF SERVOSWITCHES BY MEASURING CURRENT**

BLOCK II CONTROLLER
TECHNICAL OVERVIEW

SECTION 1 - INPUT ELECTRONICS

SECTION 2 - DIGITAL COMPUTER UNIT

SECTION 3 - COMPUTER INTERFACE ELECTRONICS

SECTION 4 - OUTPUT ELECTRONICS

SECTION 5 - POWER SUPPLY

BLOCK II POWER SUPPLY
FUNCTIONS

- PROVIDE SOLENOID/SERVOSWITCH VOLTAGES
  - Channel A Solenoids (+29 / +16 VDC)
  - Channel A Servoswitches (+39 / +26 VDC)
  - Channel B Solenoids (+24 / +8 VDC)
  - Channel B Servoswitches (+34 / +26 VDC)
- PROVIDE CURRENT LIMITING AND SHORT CIRCUIT PROTECTION
- PROVIDE EMI PROTECTION
  - MIL-STD-461 (AS MODIFIED BY SL-E-002)
- PROVIDE MEMORY, FAILURE DATA RECORDER (FDR), AND PROCESSOR HOLD-UP FROM THE 28 VDC SOURCE IN CASE OF AC POWER LOSS/TRANSIENT
- PROVIDE MEMORY AND FDR HOLD-UP FROM THE BATTERY BACK-UP IN CASE OF AC AND DC POWER FAILURE
- PROVIDE A HOLD-UP OF THE REGULATED OUTPUTS FOR 100 uSEC WHILE POWERING DOWN

BLOCK II POWER SUPPLY
FUNCTIONS

- PROVIDE OVERVOLTAGE PROTECTION FOR 5 VDC OUTPUTS
- PROVIDE A HOT-SPOT TEMPERATURE SENSOR
- PROVIDE INPUT / OUTPUT POWER ISOLATION
- PROVIDE SECONDARY VOLTAGE POWER MONITORING
- PROVIDE SEQUENCING CONTROL SIGNALS (STARTUP/SHUTDOWN)

BLOCK II POWER SUPPLY
FUNCTIONAL BLOCKS

- BLOCK II CONTROLLER POWER SUPPLY ELECTRONICS IS DIVIDED INTO THE FOLLOWING FUNCTIONAL BLOCKS
  - INPUT TRANSFORMER
    - CONTAINS A 3-Ø TRANSFORMER WITH BALANCED LOADING ON ALL PHASES
    - PROVIDES MAXIMUM 550 WATTS PER CHANNEL
    - GAPPED CORE CONTROLS IN-RUSH CURRENT
  - PULSE WIDTH MODULATOR AND FILTER
    - CONTAINS AN AUDIO FILTER FOR EMI SUPPRESSION
    - CONTAINS +5 VDC LOGIC CURRENT LIMITING
    - DRIVES THE DC - DC CONVERTOR

BLOCK II POWER SUPPLY
FUNCTIONAL BLOCKS

- POST REGULATORS (SECONDARY REGULATORS)
  - PROVIDE PRECISION VOLTAGE REGULATION
  - PROVIDES +5 VDC DIODE 'OR' LOGIC (NON-INTERRUPTABLE)
  - PROVIDE SHORT CIRCUIT PROTECTION

- DC HOLD-UP SUPPLY
  - PROVIDES +5 VDC SOURCE TO POST REGULATORS FOR DIODE 'OR'
  - PROVIDES +15 VDC SIGNAL TO OE FOR 28 VDC MONITORING
  - TRANZORB PROTECTION FOR HIGH VOLTAGE TRANSIENTS

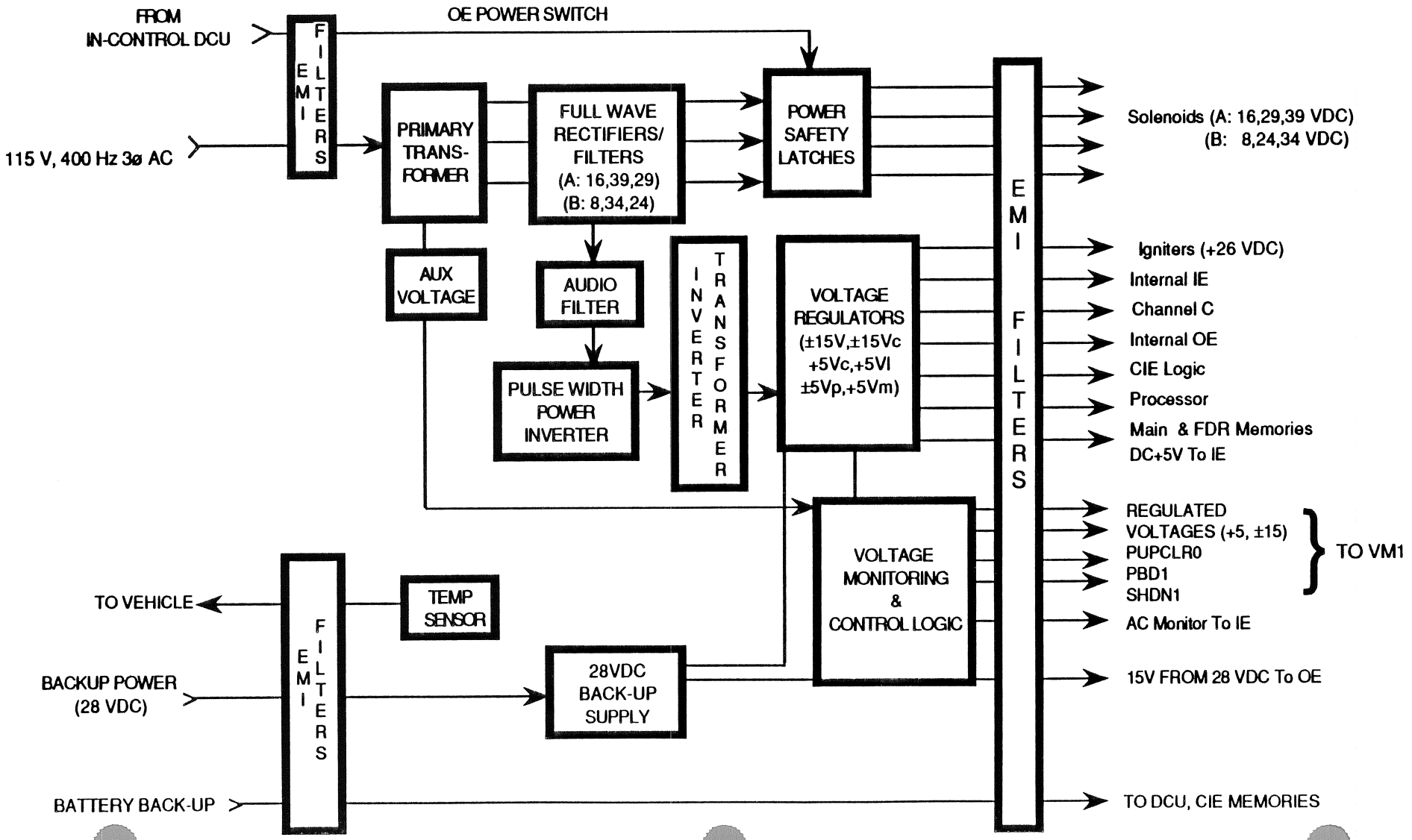
- POWER SUPPLY MONITOR
  - MONITORS STATUS OF ALL EXTERNAL VOLTAGES
  - MONITORS STATUS OF ALL INTERNAL VOLTAGES
  - PROVIDES FOR STARTUP / SHUTDOWN CONTROL SEQUENCING

BLOCK II POWER SUPPLY
FUNCTIONS BY MODULE/CARD

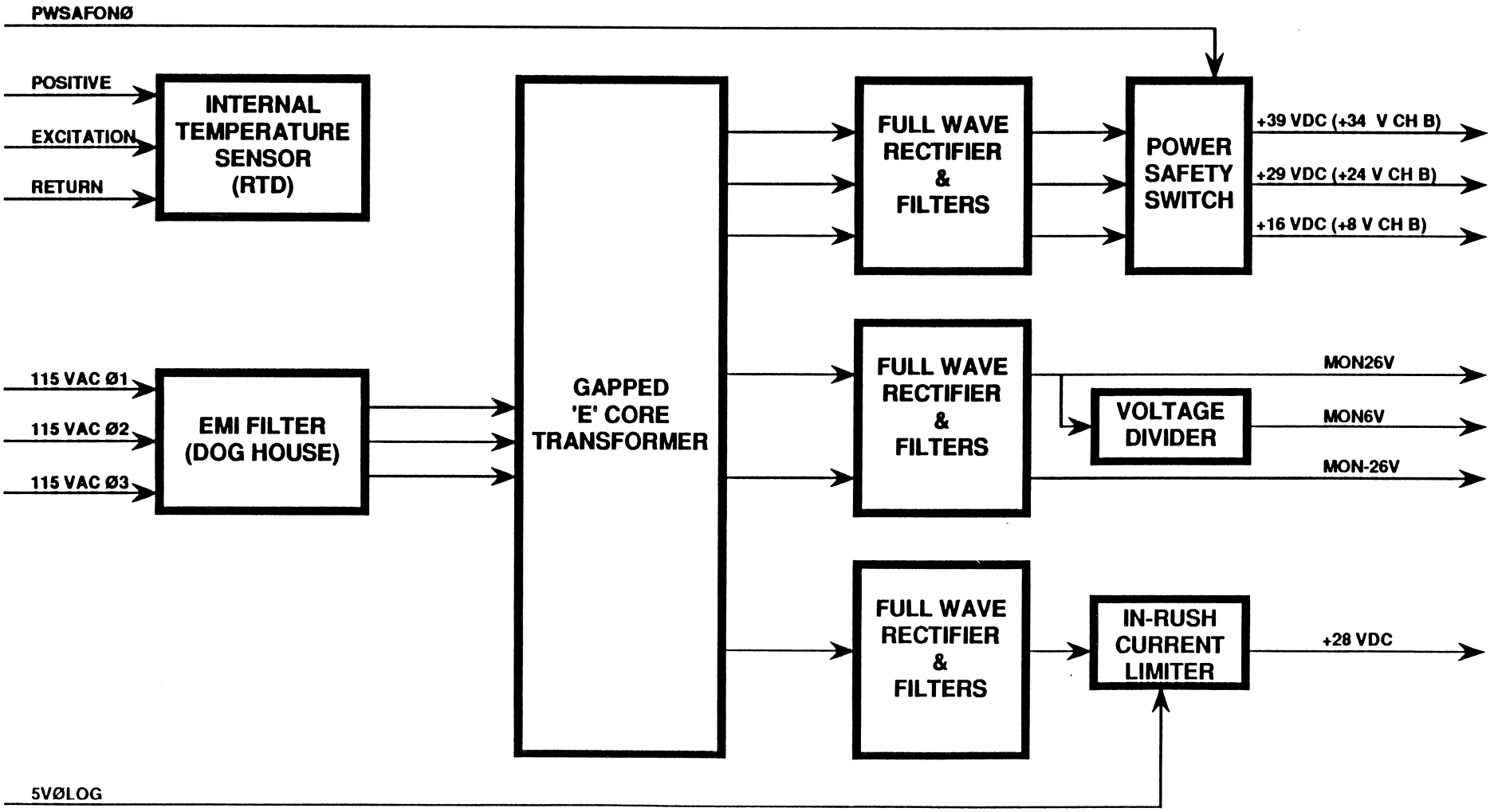
- THE BLOCK II POWER SUPPLY CONSISTS OF TEN MODULES PER CHANNEL
  - CHANNEL A FUNCTIONS ARE ON MODULES A1 THRU A10
  - CHANNEL B FUNCTIONS ARE ON MODULES A11 THRU A20

FUNCTIONS	MODULE
INPUT TRANSFORMER	A1 / A11
AUDIO FILTER	A2 / A12
OUTPUT TRANSFORMER	A3 / A13
+28 VDC HOLD-UP	A4 / A14
+5 VDC OUTPUT	A5 / A15
+15 VDC OUTPUT	A6 / A16
+26 VDC OUTPUT	A7 / A17
POWER MONITOR 1	A8 / A18
POWER MONITOR 2	A9 / A19
POWER MONITOR 3	A10 / A20

POWER SUPPLY ELECTRONICS



POWER SUPPLY
INPUT TRANSFORMER



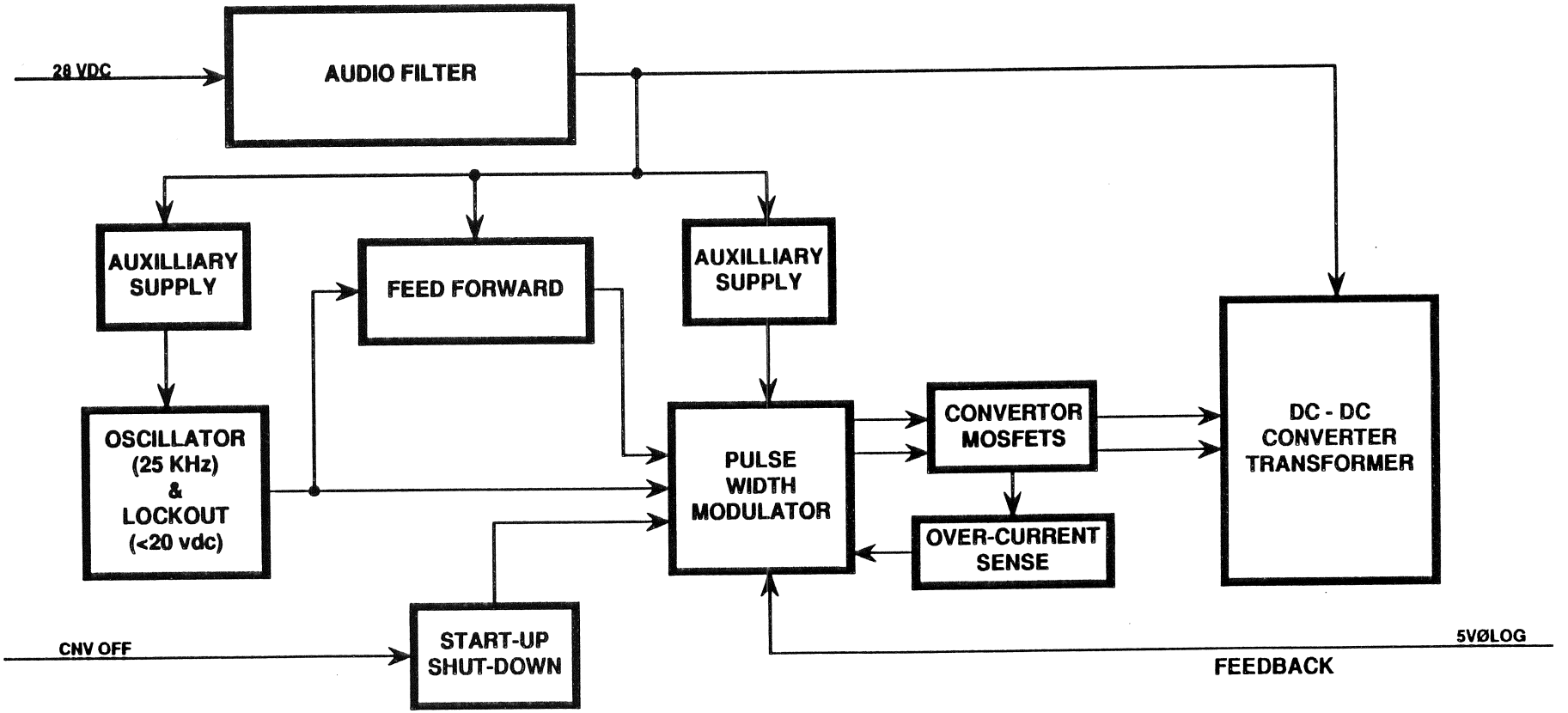
BLOCK II POWER SUPPLY
INPUT TRANSFORMER

- EMI FILTER (DOG HOUSE)
  - 3-PHASE, 400 Hz EMI FILTER
  - TRANSORBS FOR VOLTAGE SPIKE PROTECTION
- 3-PHASE INPUT TRANSFORMER
  - GAPPED 'E' CORE FOR IN-RUSH CURRENT CONTROL
  - MULTI-VOLTAGE TAPPED OUTPUT
  - 550 WATTS MAX POWER CAPABILITY
- RECTIFIERS / FILTERS
  - FULL WAVE RECTIFIERS (2400 Hz RIPPLE)
  - SOLENOID VOLTAGES
  - MONITORING OPERATING VOLTAGES
  - 28 VDC FOR THE DC - DC CONVERTER

BLOCK II POWER SUPPLY
INPUT TRANSFORMER

- IN-RUSH CURRENT LIMITER
  - ADDS SERIES RESISTANCE TO THE 28 V
  - LIMITS RATE OF CHANGE OF 28 V TO DC - DC CONVERTER UPON POWER-UP
  - RESISTORS ARE SHUNTED OUT ONCE THE INPUT FILTERS ARE CHARGED
- RESISTANCE TEMPERATURE DEVICE (RTD)
  - 100 Ω DEVICE LOCATED ON THE TRANSFORMER
  - MONITORS THE WARMEST SPOT IN THE CONTROLLER
- POWER SAFETY SWITCH
  - PULLS POWER TO SOLENOIDS BASED UPON INPUT FROM THE OE (PWSAFONØ)

POWER SUPPLY
PULSE WIDTH MODULATOR



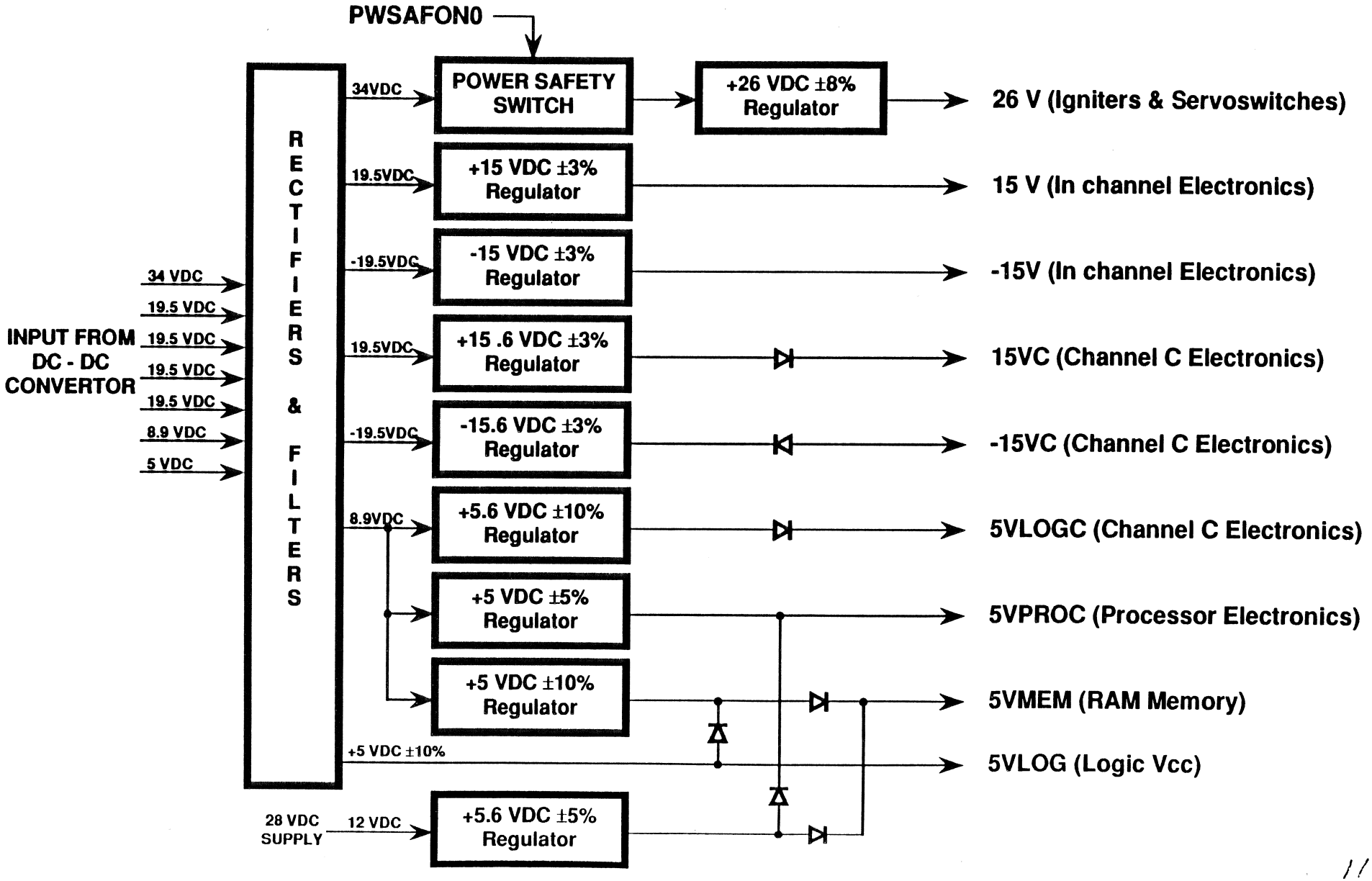
BLOCK II POWER SUPPLY
PULSE WIDTH MODULATOR

- AUDIO FILTER
    - MULTI-STAGE LC FILTER
    - PREVENTS AUDIO NOISE FROM ENTERING / EXITING THE POWER SUPPLY
    - PROVIDE A SECONDARY SOURCE OF ENERGY TO MAINTAIN CONTROLLER VOLTAGES FOR 100 uS AFTER AC POWER-OFF
- OSCILLATOR AND LOCKOUT
    - ESTABLISHES THE PULSE WIDTH MODULATOR (PWM) FREQUENCY AT 25 KHz (SQUARE WAVE)
    - TURNS OFF THE PWM IF THE 28 VOLT SOURCE DROPS BELOW 20 V
- PULSE WIDTH MODULATOR
    - MAINTAINS A CONSTANT VOLTAGE OUT OF THE DC - DC CONTERTOR
        - ADJUSTS DUTY CYCLE OF 25 KHz SQUARE WAVE TO MAINTAIN CONSTANT +5 VOLT LOGIC
        - 5VØLOG IS USED FOR FEEDBACK CONTROL (FLUCTUATES DEPENDING ON SYSTEM DRAW)

BLOCK II POWER SUPPLY
PULSE WIDTH MODULATOR

- START-UP / SHUT-DOWN
  - CONTROLS THE PWM CIRCUIT BASED UPON A SIGNAL FROM THE P/S MONITOR
- DC - DC TRANSFORMER
  - TOROIDAL TRANSFORMER WITH CENTER TAPPED PRIMARY & MULTI-TAPPED SECONDARY
- FEED FORWARD
  - IMPROVES DYNAMIC REGULATION TO INPUT VARIATIONS
  - FUNCTIONS AS PRE-REGULATOR TO CORRECT FOR AMPLITUDE VARIATION IN THE 115 VAC INPUT
  - REDUCES VARIATION OF +5 VOLT LOGIC SUPPLY

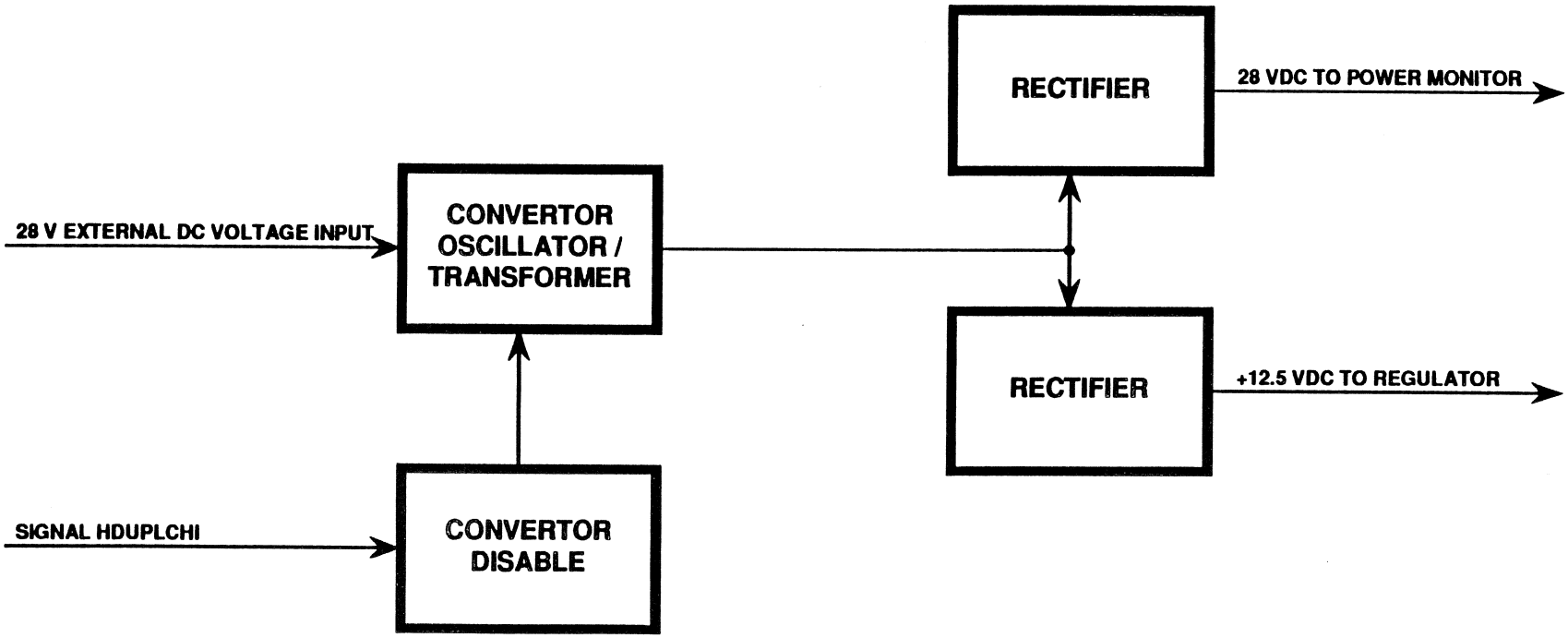
POWER SUPPLY
POST REGULATORS



BLOCK II POWER SUPPLY
POST REGULATORS

- RECTIFIERS AND FILTERS
  - FULL WAVE RECTIFICATION OF 25 KHz SQUARE WAVE FROM DC - DC CONVERTOR
  - FILTERS CURRENT AND VOLTAGE VARIATIONS
- POST REGUALTORS
  - PERFORMS FINAL ADJUSTMENT OF ENGINE AND CONTROLLER VOLTAGE LEVELS
- DOIDE 'OR'
  - +5 VOLT REGULATED SOURCE TO MEMORY AND PROCESSOR DIODE 'OR' WITH ORBITER SUPPLIED 28 VOLTS
  - +5 VOLT LOGIC SOURCE (UNREGULATED) DOIDE 'OR' WITH +5 VOLTS TO MEMORY

POWER SUPPLY
28 VOLT BACKUP SUPPLY



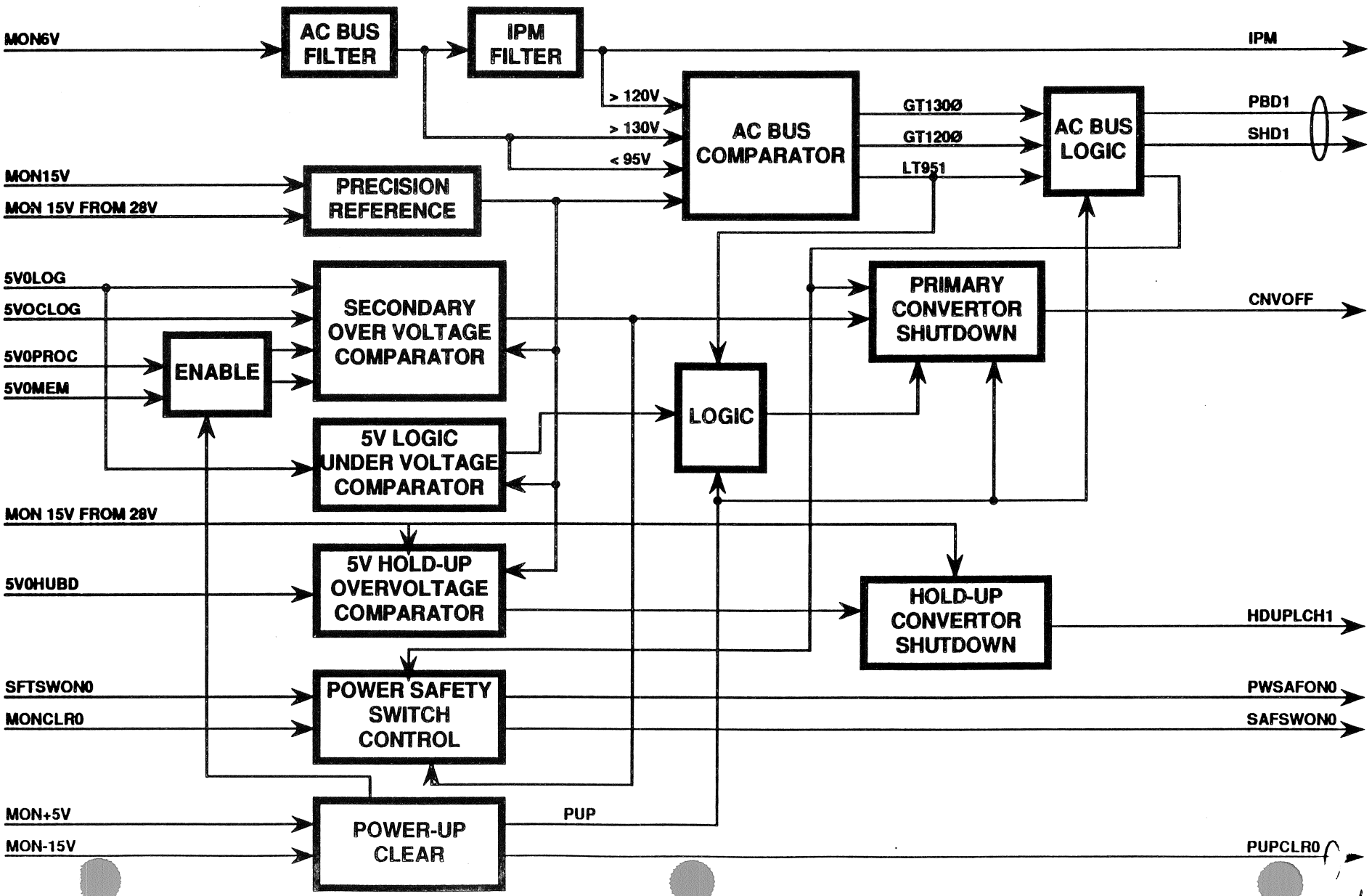
BLOCK II POWER SUPPLY
28 VDC BACK-UP SUPPLY

- CONVERTOR OSCILLATOR / TRANSFORMER
  - PROVIDES ISOLATION OF 28 VDC SUPPLY FROM CONTROLLER ELECTRONIC
  - OSCILLATOR DRIVES PRIMARY OF TRANSFORMER (SQUARE WAVE)
  - PROVIDES DRIVE FOR FULL WAVE RECTIFIERS
- CONVERTOR DISABLE
  - SHUTS DOWN THE BACKUP SUPPLY WHENEVER +5VMEM AND +5VPROC EXCEED LIMIT
    - HDUPLCHI IS PROVIDED BY THE POWER SUPPLY MONITOR OVER VOLTAGE CIRCUIT
- RECTIFIERS
  - FULL WAVE RECTIFICATION OF TRANSFORMER OUTPUT (SQUARE WAVE)

BLOCK II POWER SUPPLY
POWER SUPPLY MONITORS

- THERE ARE TWO AREAS OF THE POWER SUPPLY MONITOR
  - INBOARD CHASSIS MONITOR
    - MONITORS PRIMARILY INCOMING VOLTAGES AND CURRENT
  - MAIN CHASSIS ELECTRONICS MONITOR - VOLTAGE MONITOR ASSEMBLY (VMI)
    - PROVIDES PROPER SEQUENCING ON AND OFF FOR THE CONTROLLER ELECTRONICS

POWER SUPPLY
INBOARD CHASSIS POWER MONITOR



BLOCK II POWER SUPPLY
INBOARD CHASSIS MONITOR

- AC BUS FILTER
  - PROVIDES AC DERIVED 5.85V FOR COMPARISON TO PRECISION REFERENCE 5.85V
- IPM FILTER
  - PROVIDES AC DERIVED 2.5V FOR COMPARISON TO PRECISION REFERENCE 2.5V
- AC BUS COMPARATOR
  - COMPARES AC DERIVED 5.85V TO PRECISION REFERENCE
    - DETECTS GREATER THAN 130 VAC
    - DETECTS LESS THAN 95 VAC
  - COMPARES AC DERIVED 2.5V TO PRECISION REFERENCE
    - DETECTS GREATER THAN 120 VAC

BLOCK II POWER SUPPLY
INBOARD CHASSIS MONITOR

- SECONDARY OVER VOLTAGE COMPARATOR
  - COMPARES DERIVED VOLTAGES TO PRECISION REFERENCE
    - +5 VOLT LOGIC (5V0LOG) - SHUTDOWN IF < 5.92 VDC
    - +5 VOLT CHANNEL C LOGIC (5V0CLOG) - SHUTDOWN IF < 5.92 VDC
    - +5 VOLT PROCESSOR SUPPLY (5V0PROC) - SHUTDOWN IF < 5.92 VDC (AC AND 28 VDC 'OR' POWER)
    - +5 VOLT MEMORY SUPPLY (5V0MEM) - SHUTDOWN IF < 5.92 VDC (AC AND 28 VDC 'OR' POWER)
- 5 VOLT LOGIC UNDER VOLTAGE COMPARATOR
  - COMPARES AC DERIVED LOGIC VOLTAGE TO PRECISION REFERENCE
    - SHUTDOWN IF < 4.0 V

BLOCK II POWER SUPPLY
INBOARD CHASSIS MONITOR

- 5 VOLT HOLD-UP OVER VOLTAGE COMPARATOR
  - COMPARES 28 VDC DERIVED +5 V HOLD-UP TO PRECISION REFERENCE
- HOLD-UP CONVERTOR SHUTDOWN
  - SHUTDOWN HOLD-UP DC - DC CONVERTOR IF +5 V HOLD-UP > 5.9 V
    - APPLIES 15 VDC TO OPTICAL COUPLER WHICH CONTROLS DC - DC CONVERTOR
- AC BUS LOGIC
  - ISSUE POWER BUS DOWN (PBD1), SHUTDOWN (SHD1) AND CONVERTOR SHUTDOWN ON COMMAND FROM THE AC BUS COMPARATOR
    - SHUTS DOWN IMMEDIATELY IF GREATER THAN 130 VAC DETECTED
    - SHUTS DOWN IMMEDIATELY IF LESS THAN 95 VAC DETECTED
    - SHUTS DOWN AFTER 20 mS IF GREATER THAN 120 VAC DETECTED

BLOCK II POWER SUPPLY
INBOARD CHASSIS MONITOR

- PRIMARY CONVERTOR SHUTDOWN
  - ISSUES CONVERTOR SHUTDOWN (CNVOFF1)
    - UPON AN AC BUS OR SECONDARY REGULATOR OVERVOLTAGE
    - 100 uS AFTER AN AC BUS UNDERVOLTAGE
    - UPON A 5 VOLT LOGIC (5V0LUV0) UNDERVOLTAGE
- POWER SAFETY SWITCH CONTROL
  - ISSUES POWER SAFETY SWITCH ON (PWSAFON0) UPON
    - A SECONDARY SUPPLY OVERVOLTAGE
    - AC BUS OVERVOLTAGE
    - LOSS OF OPERATING VOLTAGES (MONCLR0)

BLOCK II POWER SUPPLY
INBOARD CHASSIS MONITOR

- POWER UP CLEAR
    - RESETS ALL CIRCUITS UPON POWER UP
- LOGIC
    - DELAY/LOGIC CIRCUITS FOR CONVERTOR SHUTDOWN (100 uS)

BLOCK II POWER SUPPLY
VOLTAGE MONITOR ASSEMBLY (VMI)

- DELAY TIMERS
  - PROVIDE 100 mS DELAY PRIOR TO ENABLING CONTROLLER ELECTRONICS
  - PROVIDE 1.25 uS RESET TIMER TO POWER ON / OFF LOGIC
    - MONITOR CLEAR (MONCLR0), CLEAR0, RESET0, MEMORY SAVE (MEMSAVE1)
- POWER ON / OFF LOGIC
  - DETECTS A POWER DOWN CONDITION
    - ALERTS CONTROLLER OF POWER DOWN CONDITION